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MS-7399

Version 1.0

CPU:

Intel Prescott (L2=2MB)
 Intel Cendar Mill (65nm)
 Intel Smithfield (90nm Dual core)
 Intel Presler (65nm Dual core)
 Intel Conroe (65nm Dual core)
 Intel Kentsfield
 Intel Yorkfield
 Intel Wolfdale

System Chipset:

nVidia - MCP73PV/S

On Board Chipset:

BIOS -- SPI FLASH 4Mb
 Azalia CODEC(ALC 888S)
 LPC Super I/O -- ITE8718F
 LAN-Realtek RTL8211BL
 IEEE1394 -- VIA VT6308P

Main Memory:

DDR II * 2 (Max 2GB)

Expansion Slots:

PCI Express X16 SLOT * 1
 PCI Express X1 SLOT * 1
 PCI 2.3 SLOT * 2

Intersil PWM:

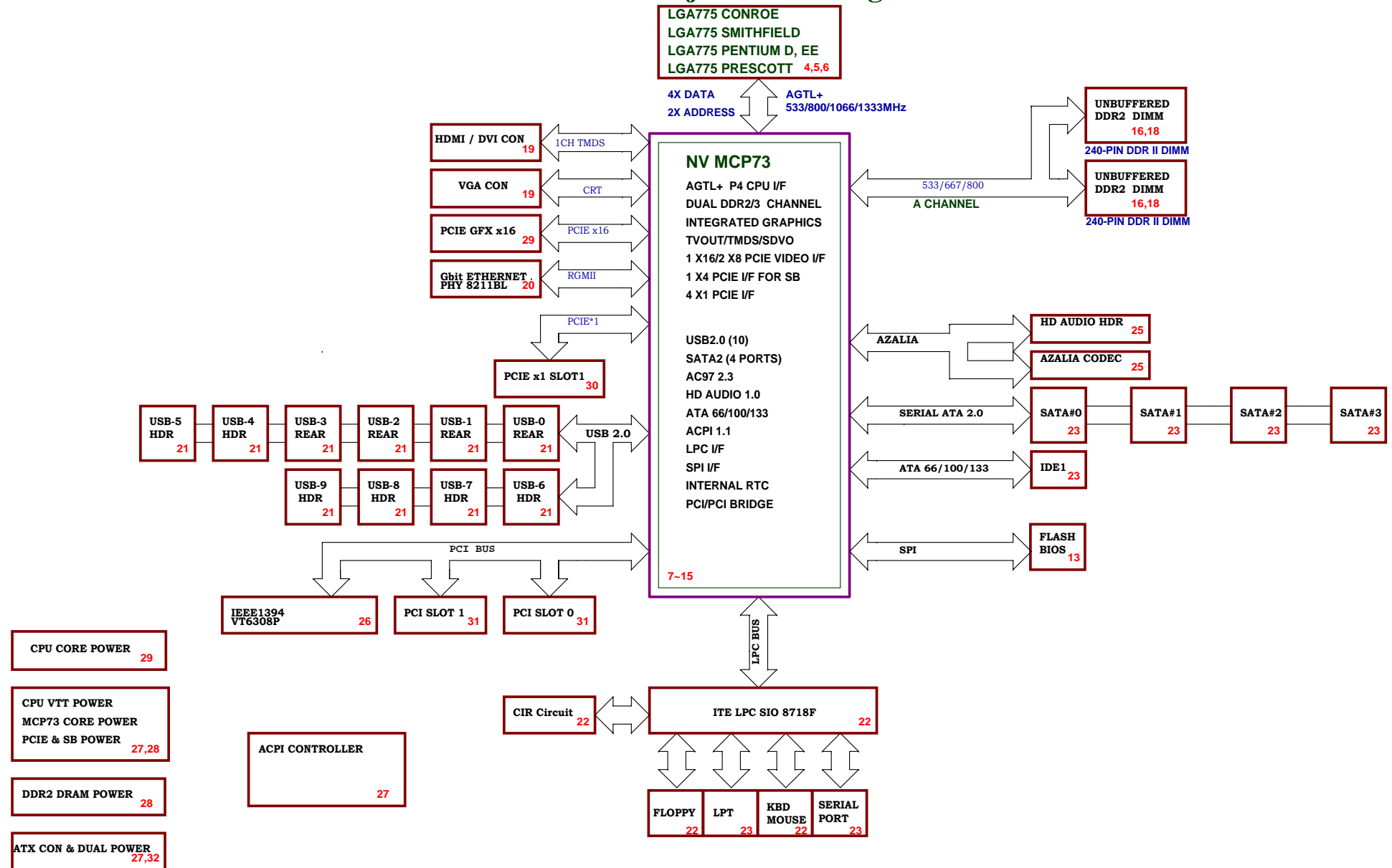
Controller: Intersil 6312 3 Phase



Persian Project

Aspire M5640/M3640
 HDMI + 1394

acer Persian Project Block Diagram



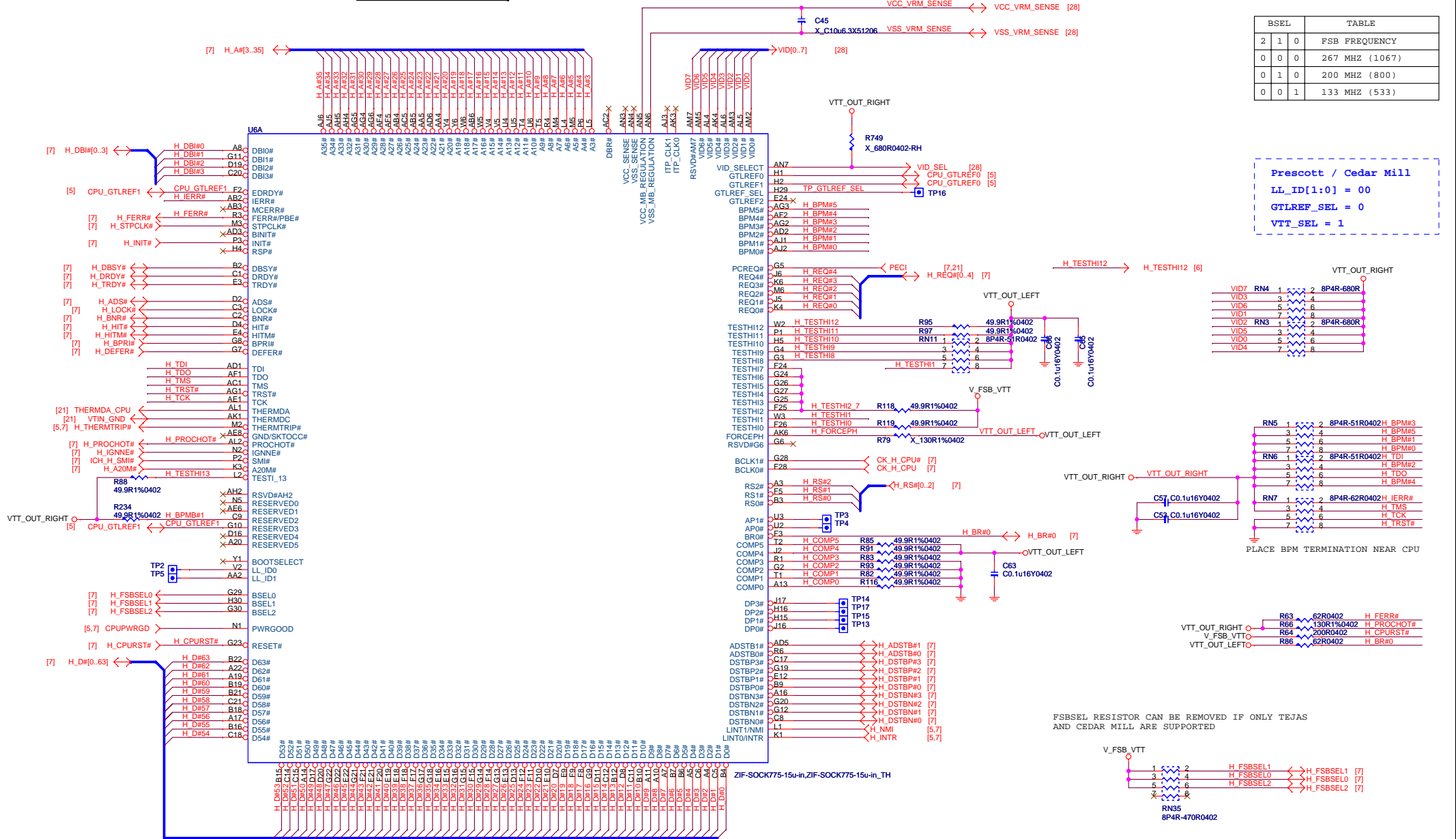
MCP73 GPIO Config.

GPIO Pin	Type	Primary State
GPIO_2/NMI/PS2_CLK0	I/O(S5_3.3V)	TMDS_DET1
GPIO_3/SMI#/PS2_DATA0	I/O(S5_3.3V)	TMDS_DET2
GPIO_4/SCI/INTR/PS2_CLK1	I/O(S5_3.3V)	Unused
GPIO_5/INIT#/PS2_DATA1	I/O(S5_3.3V)	OBR1
GPIO_6/FERR#/SYS_SERR#/IGPU_GPIO6	I/O(S5_3.3V)	Unused
GPIO_7/NFERR#/SYS_PERR#/IGPU_GPIO7	I/O(S5_3.3V)	Unused
GPIO_8/SPI_DI	I/O(S5_3.3V)	Unused
GPIO_9/SPI_DO	I/O(S5_3.3V)	Unused
GPIO_10/SPI_CS0	I/O(S5_3.3V)	Unused
GPIO_11/SPI_CLK	I/O(S5_3.3V)	Unused
LPC_DRQ1#/GPIO_19/FANRPM1	I/O(3.3V)	Unused
PROCHOT#/GPIO_20	I/O(CPU_VTT)	H_PROCHOT#
PE_WAKE#/GPIO_21	I/O(S5_3.3V)	WAKE#
HDA_SDATA_IN0/GPIO_22	I/O(S5_3.3V)	HDA_SDATA_IN
HDA_SDATA_IN1/GPIO_23/MGPIO_0	I/O(S5_3.3V)	Unused
HDA_SDATA_IN2/GPIO_24/MGPIO_2	I/O(3.3V)	Unused
USB_OC0#/GPIO_25	I/O(S5_3.3V)	OC#1
USB_OC1#/GPIO_26	I/O(S5_3.3V)	OC#2
USB_OC2#/GPIO_27	I/O(S5_3.3V)	OC#3
USB_OC3#/GPIO_28	I/O(S5_3.3V)	Pull Hi
USB_OC4#/GPIO_29	I/O(S5_3.3V)	Pull Hi
PCI_PME#/GPIO_30	I/O(S5_3.3V)	PCI_PME#
SIO_PME#/GPIO_31	I/O(S5_3.3V)	SIO_PME#
EXT_SMI#/GPIO_32	I/O(S5_3.3V)	LPC_SMI#
SUS_CLK/GPIO_34	I/O(S5_3.3V)	Unused
MII0_INTR/GPIO_35	I/O(S5_3.3V)	RGMI0_INTR#
MII0_PXER/GPIO_36/PWR_LED#	I/O(S5_3.3V)	RGMI0_RX_ER
MII0_PWRDWN/GPIO_37	I/O(S5_3.3V)	RGMI0_PREDN
PCI_REQ3#/GPIO_38/RS232_CTS#	I/O(3.3V)	PREQ#3
PCI_GNT3#/GPIO_39/RS232_RTS#	I/O(3.3V)	Unused
PCI_REQ2#/GPIO_40/RS232_DSR#	I/O(3.3V)	PREQ#2
PCI_GNT2#/GPIO_41/RS232_DTR#	I/O(3.3V)	PGNT#2
LPC_RESET#/GPIO_42	I/O(3.3V)	Unused
PCI_PERR#/GPIO_43/RS232_DCD#	I/O(3.3V)	PERR#
HDA_SYNC/GPIO_44	I/O(3.3V)	AZ_SYNC_R
HDA_SDATA_OUT/GPIO_45	I/O(3.3V)	HDA_SDATA_OUT
LPC_DRQ0#/GPIO_50	I/O(3.3V)	LPC_DRQ#0
PCI_REQ4#/GPIO52/RS232_SIN#	I/O(3.3V)	PREQ#4
PCI_GNT4#/GPIO_53/RS232_SOUT#	I/O(3.3V)	Unused
A20GATE/GPIO_55	I/O(3.3V)	A20GATE
KBRDRSTIN#/GPIO_56	I/O(3.3V)	KBRST#
SATA_LED#/GPIO_57	A(3.3V)	SATALED#
THERMTRIP#/GPIO_58	I/O(CPU_VTT)	H_THERMTRIP#
THERM#/GPIO_59	I/O(3.3V)	Unused
FANRPM0/GPIO_60	I/O(3.3V)	OBR2
FANCTL0/GPIO_61	I/O(3.3V)	AUDIO_FRONT_IO
FANCTL1/GPIO_62	I/O(3.3V)	DEPOP_GPIO
CABLE_DET_P/GPIO_63	I/O(3.3V)	ATADETO

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTX# PCI_INTY# PCI_INTZ# PCI_INTW#	PREQ#0 PGNT#0	AD21	PCICLK0
PCI Slot 2	PCI_INTY# PCI_INTZ# PCI_INTW# PCI_INTX#	PREQ#1 PGNT#1	AD22	PCICLK1
1394	PCI_INTW#	PREQ#2 PGNT#2	AD23	1394_PCLK

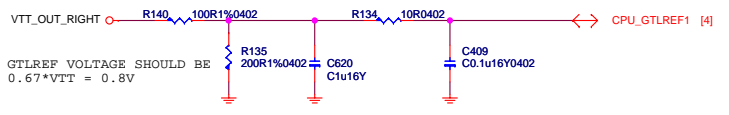
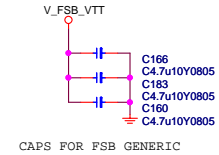
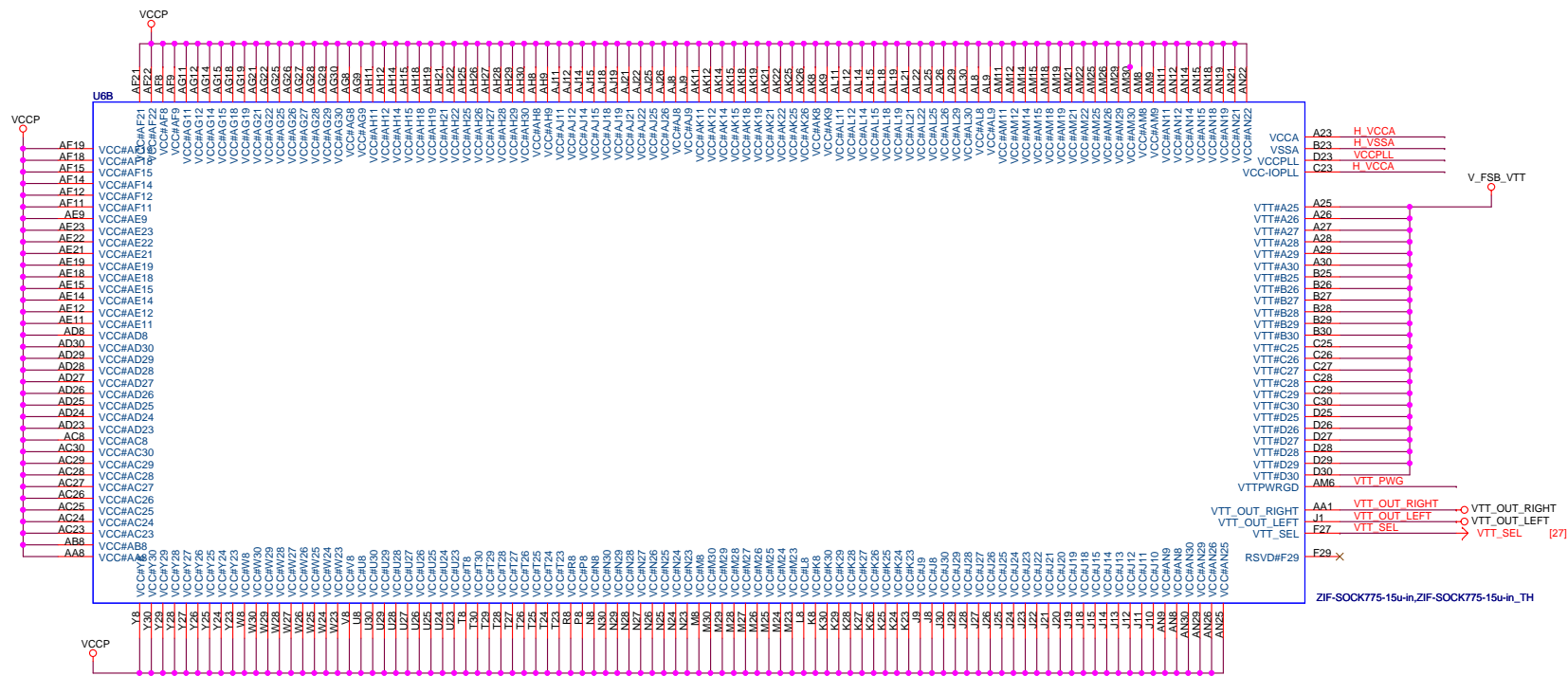
CPU SIGNAL BLOCK



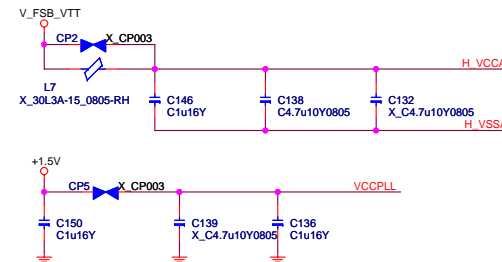
BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	267 MHZ (1067)
0 1 0	200 MHZ (800)
0 0 1	133 MHZ (533)

Prescott / Cedar Mill
 LL_ID[1:0] = 00
 GTLREF_SEL = 0
 VTT_SEL = 1

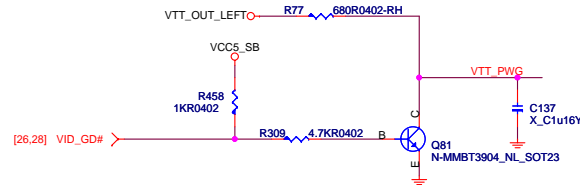
FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS AND CEDAR MILL ARE SUPPORTED

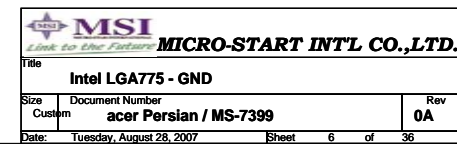


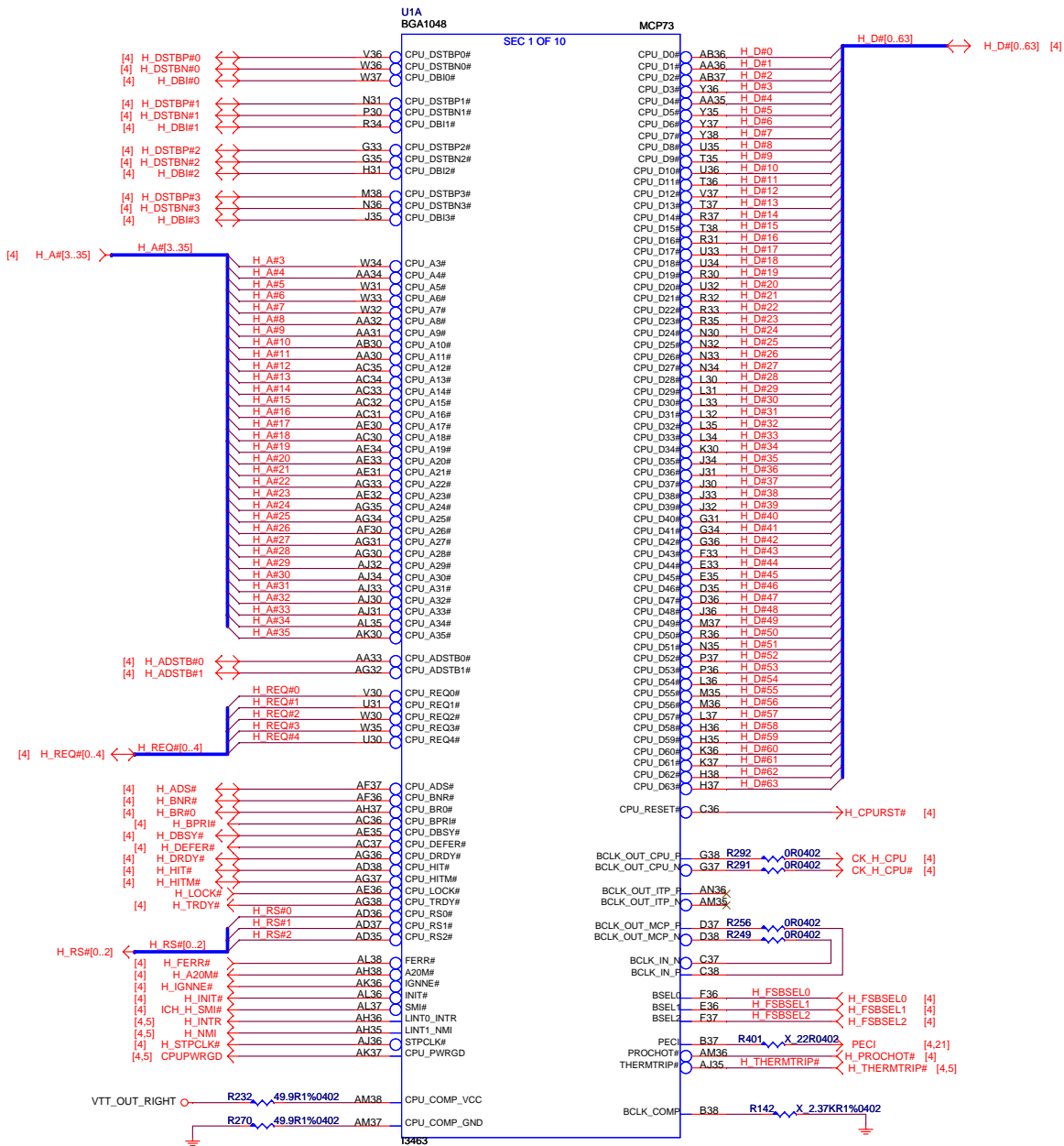
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS

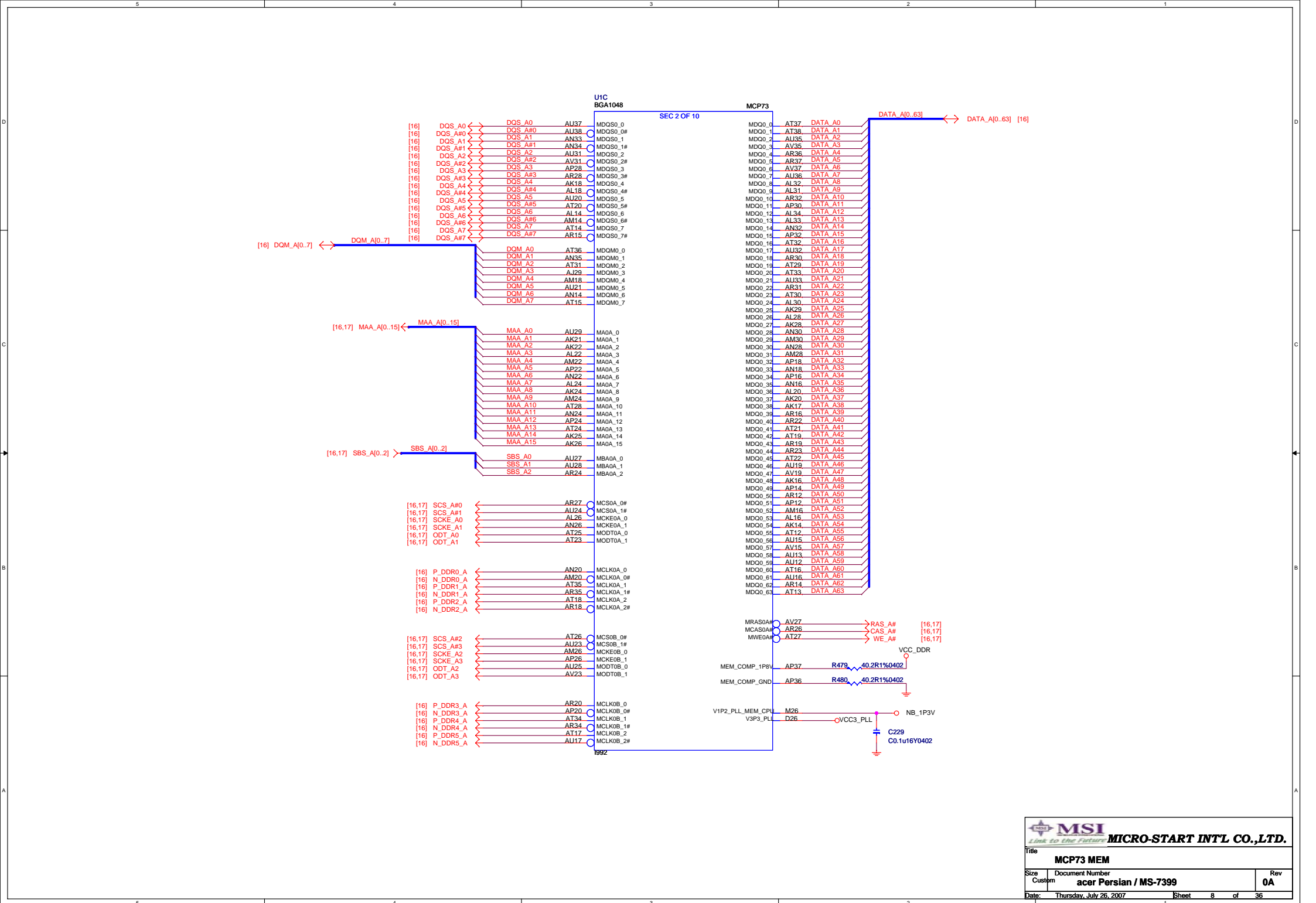


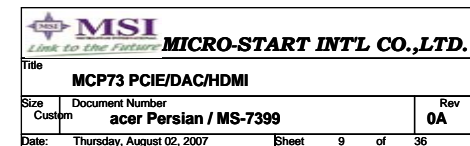
VTT_PWRGOOD

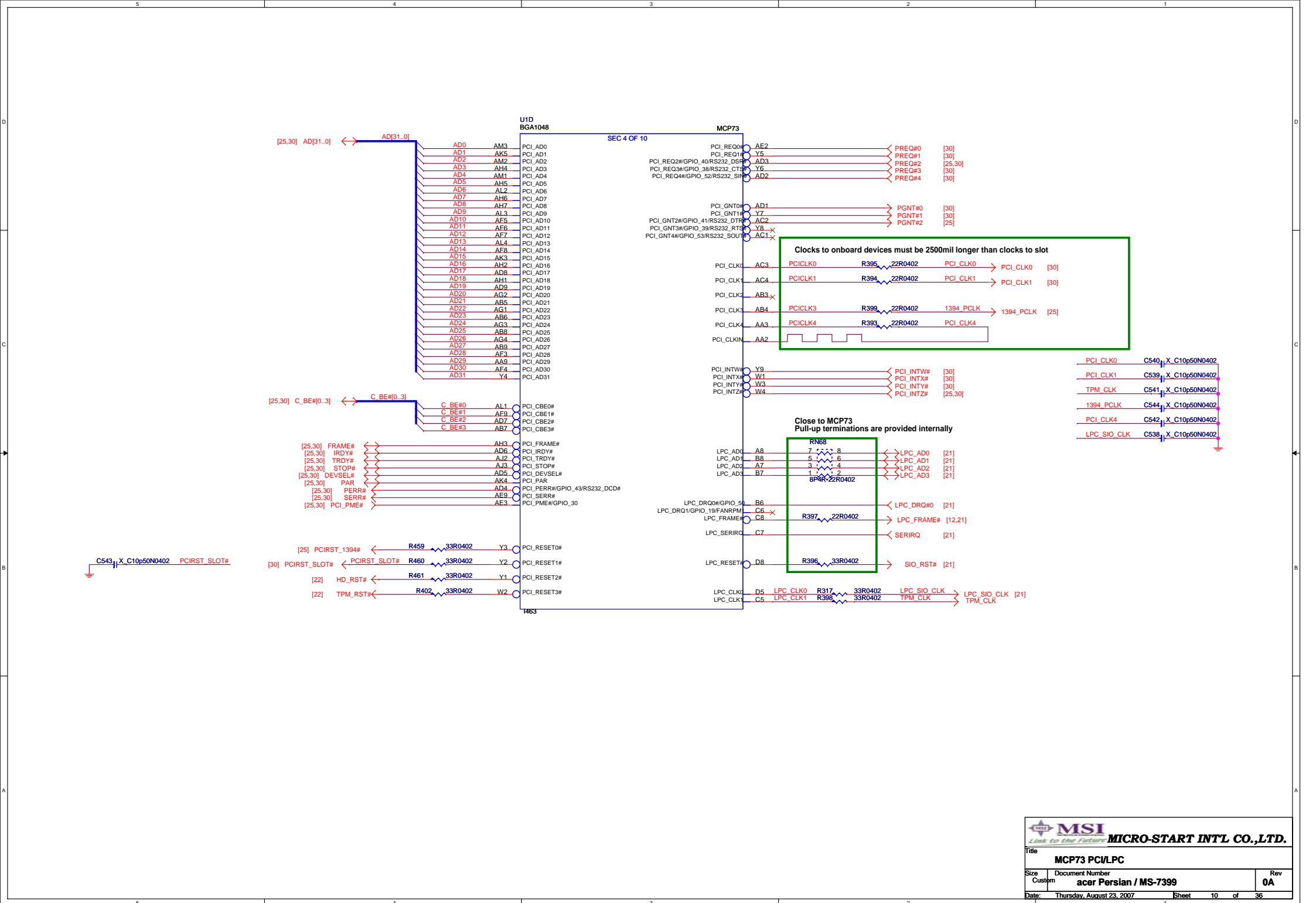


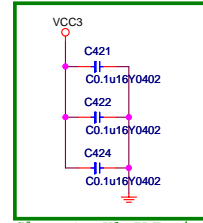
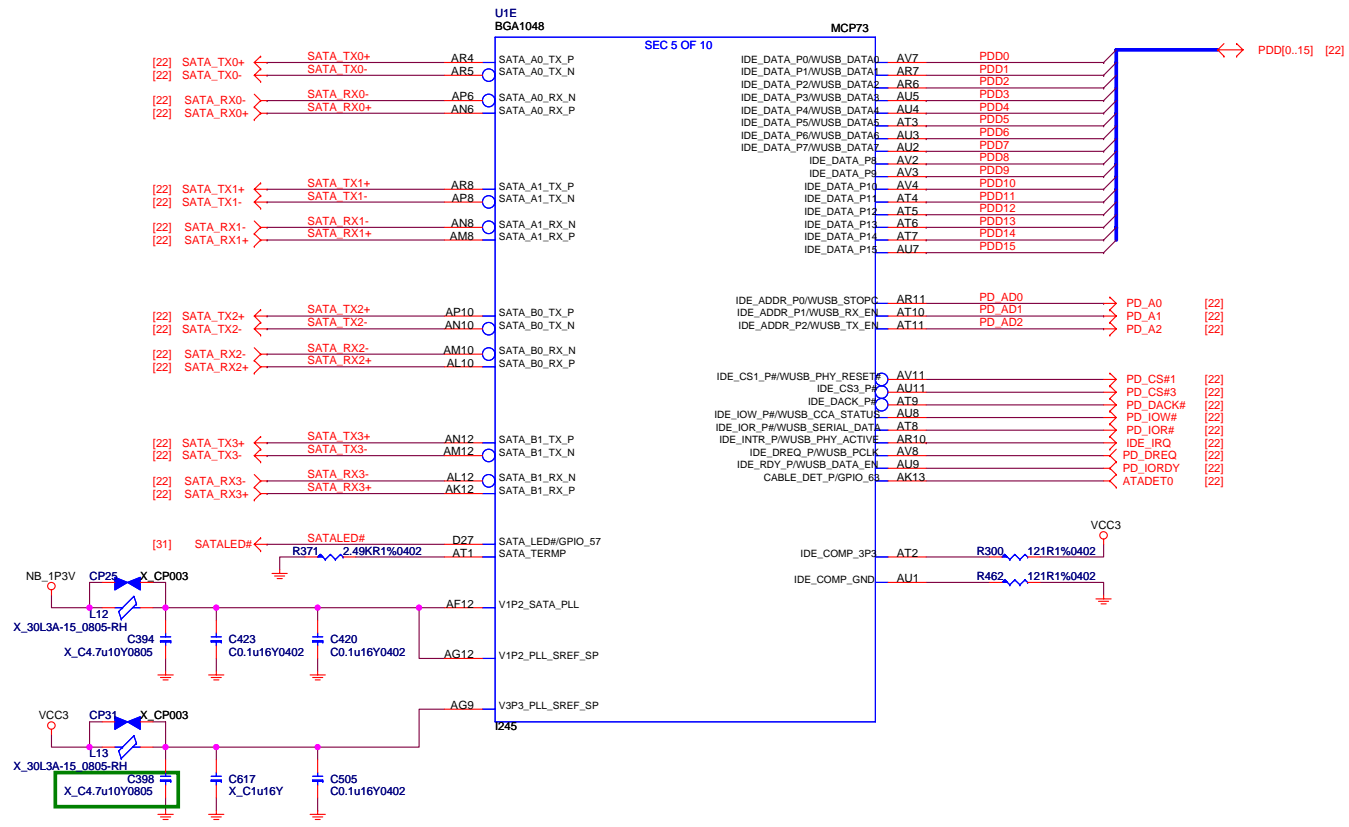






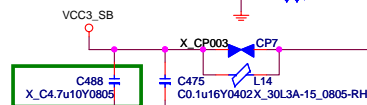
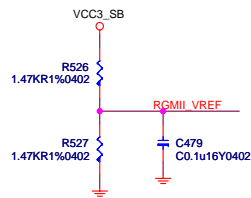
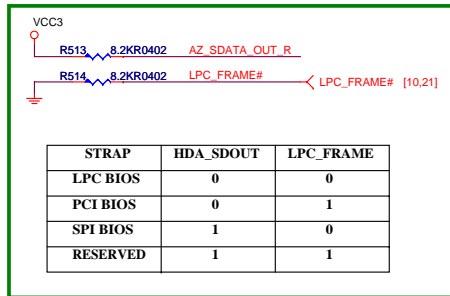
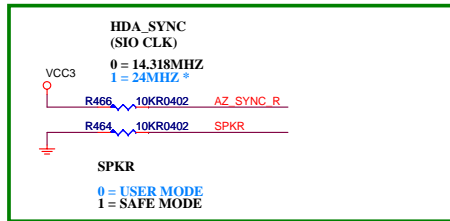
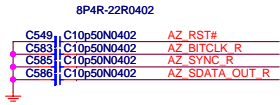
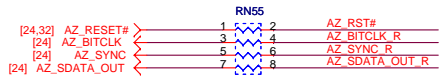
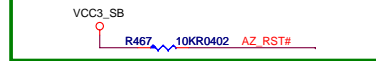




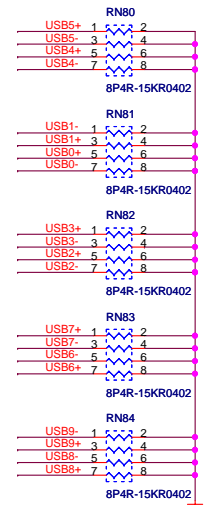
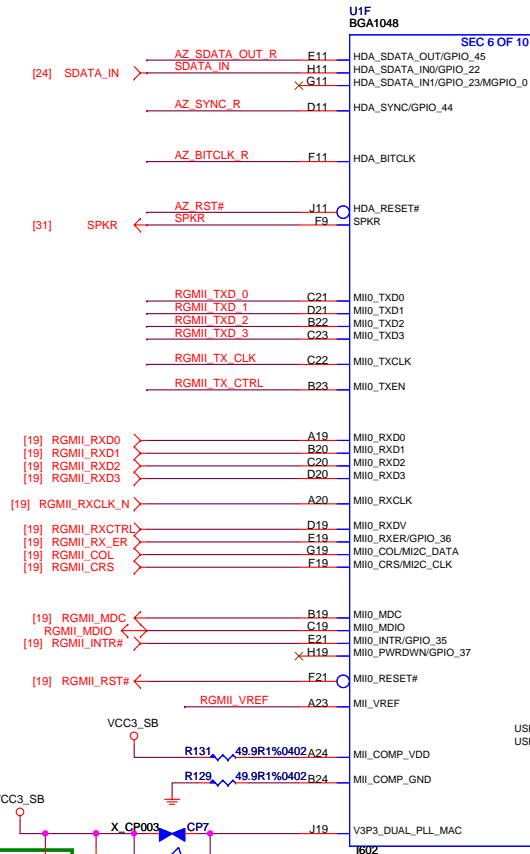
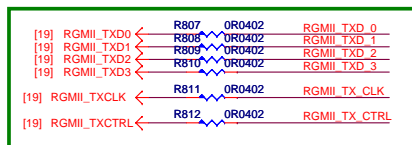


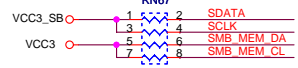
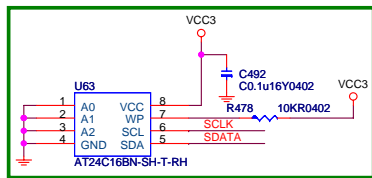
Close to U1 IDE signal balls

Strapping 10K ohm to VCC3_SB: RGMII

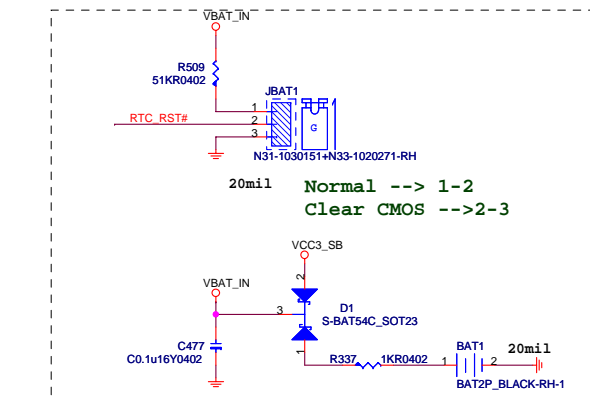
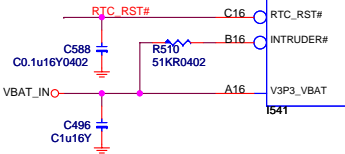
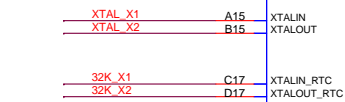
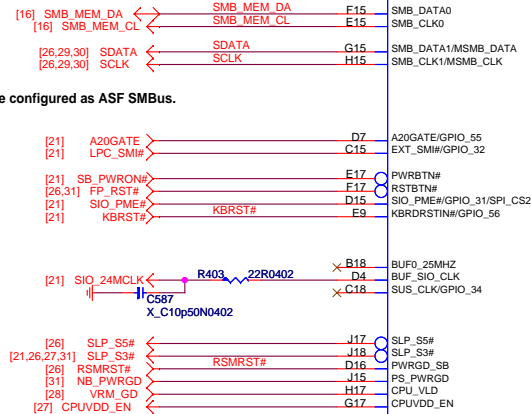
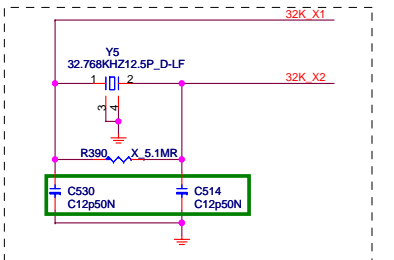
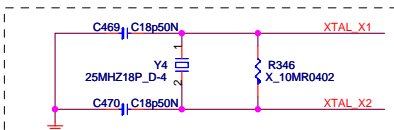
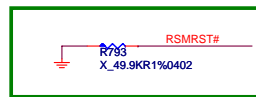
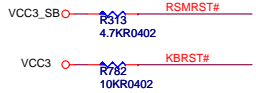


Close to U1

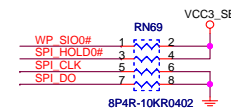
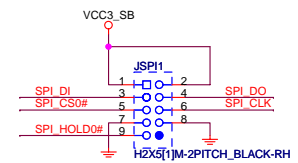
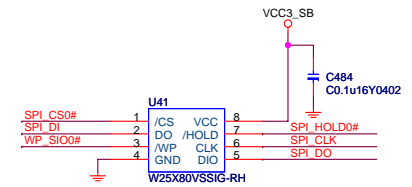
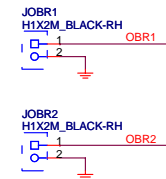
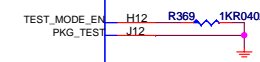
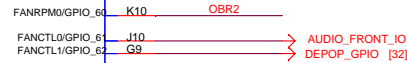
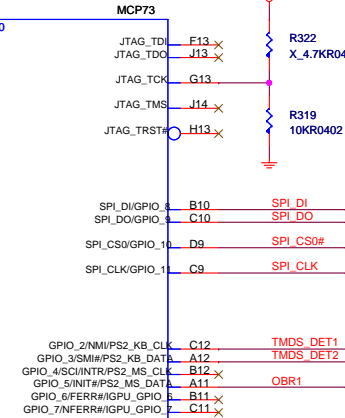




When SDATA/SCLK are not used, it can be configured as ASF SMBus.

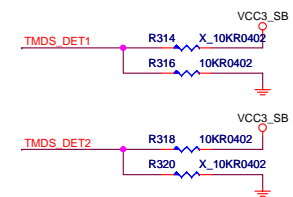


20mil Normal --> 1-2
Clear CMOS --> 2-3



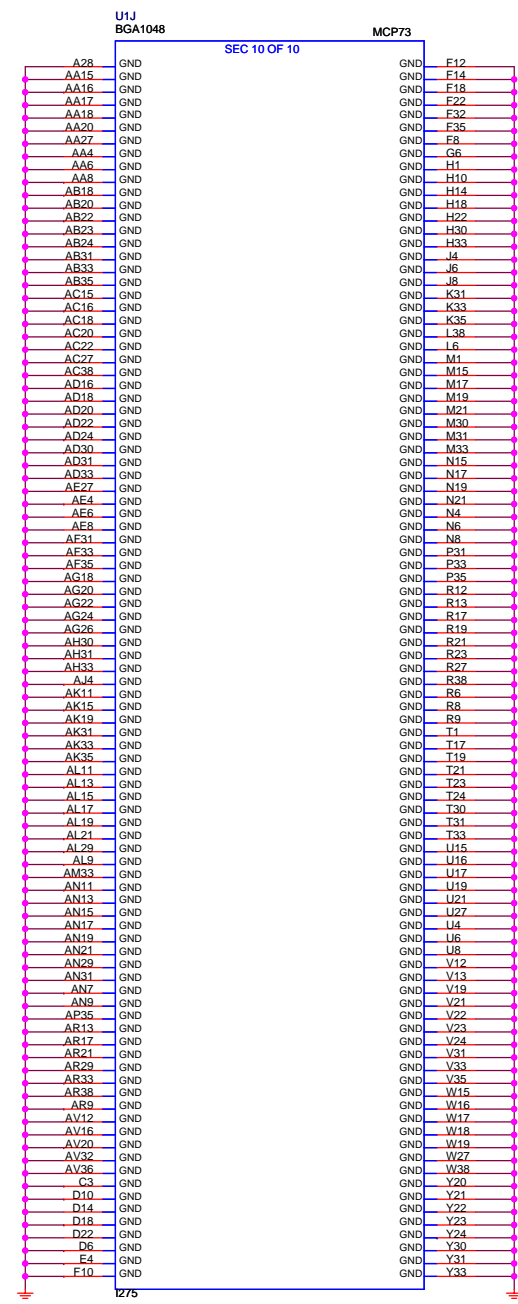
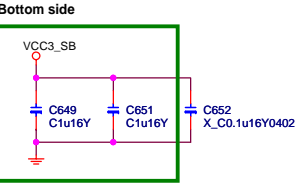
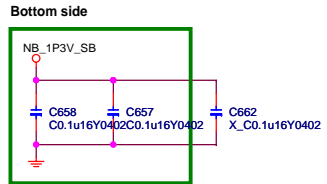
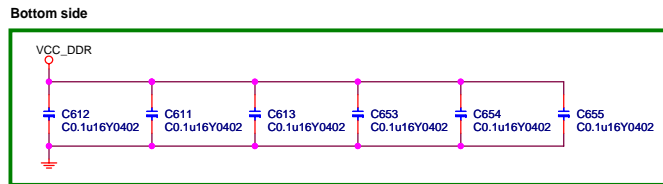
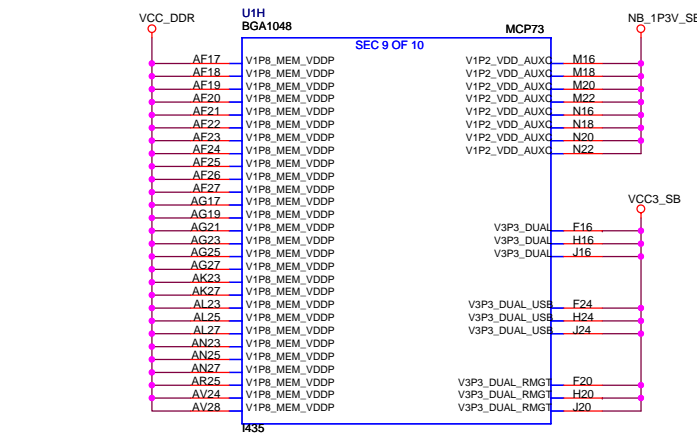
MCP73 SPI CLK STRAP

STRAP	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1



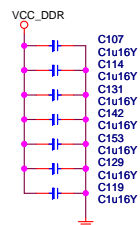
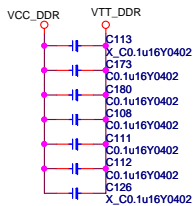
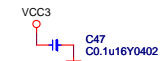
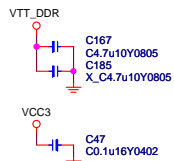
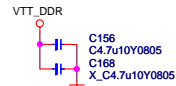
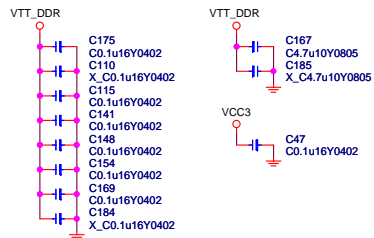
HDMI/DVI Detect

	TMDs_DET1	TMDs_DET2
DVI	1	0
HDMI	0	1
N/A	0	0

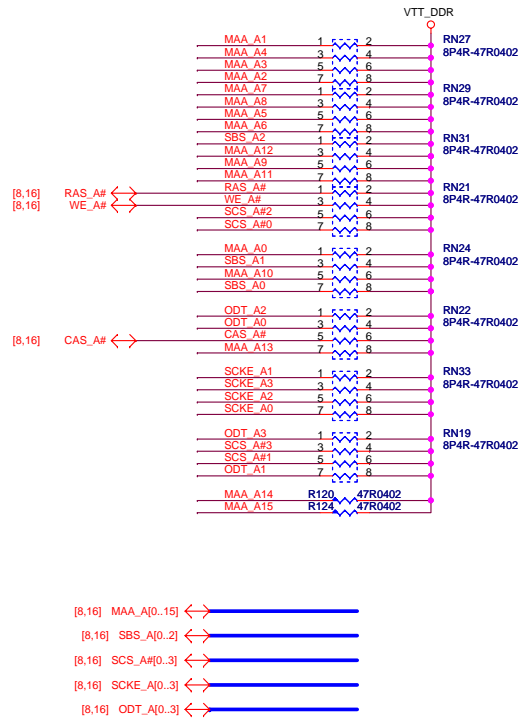


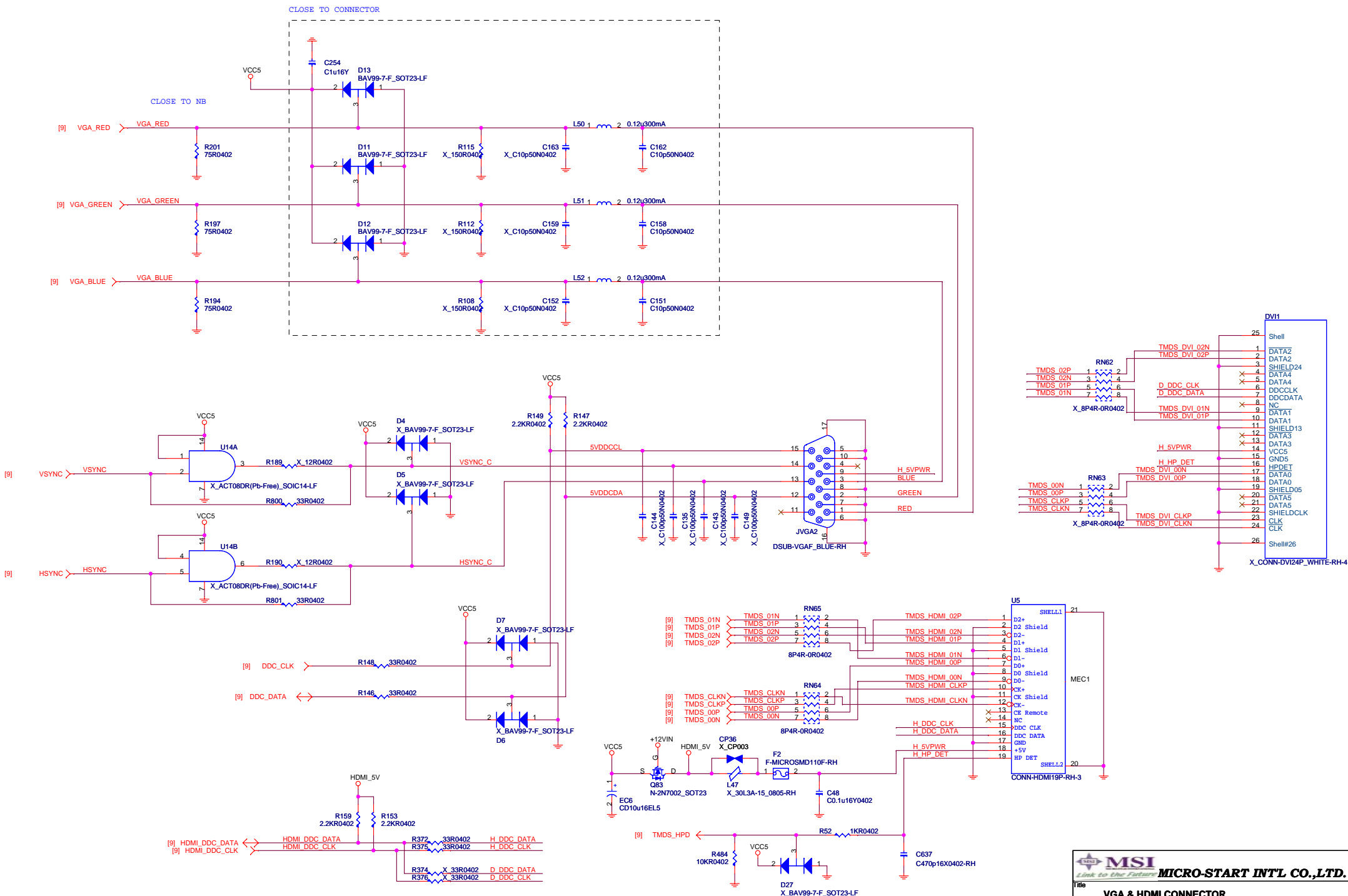


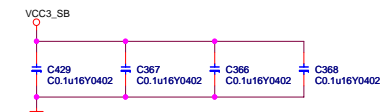
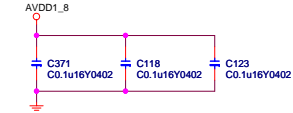
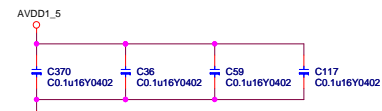
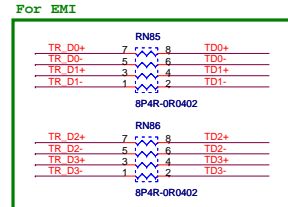
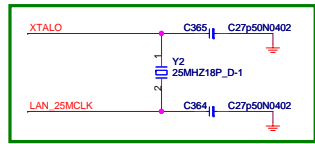
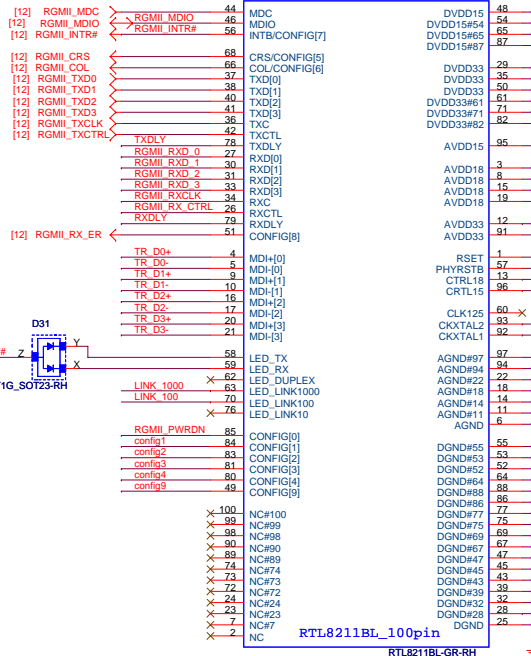
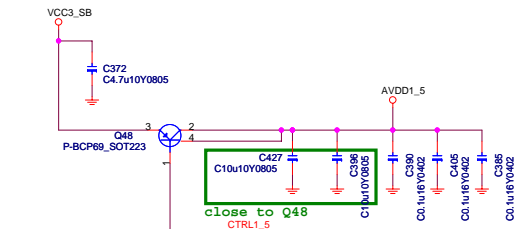
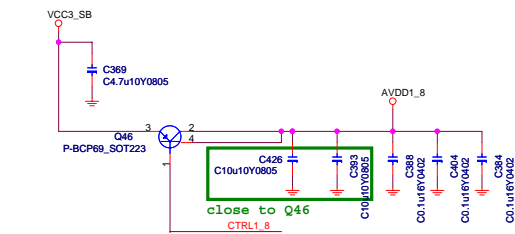
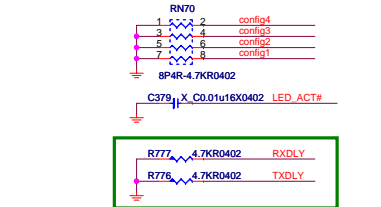
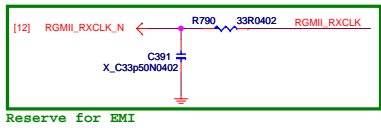
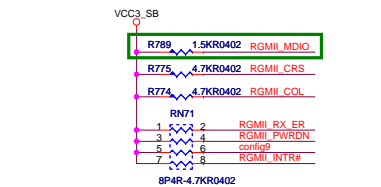
CHANNEL A VTT_DDR
DECOUPLING CAPS



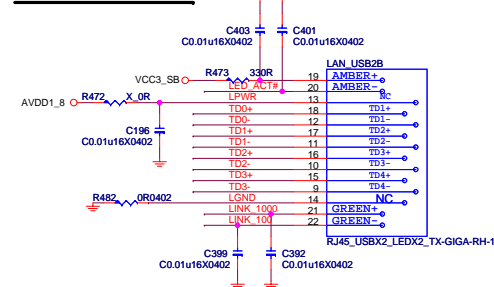
DDR II TERMINATION



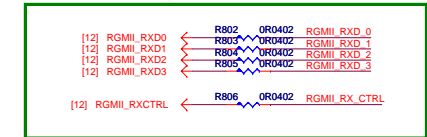




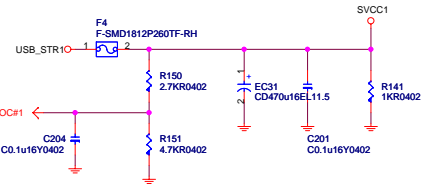
LAN CONNECTOR



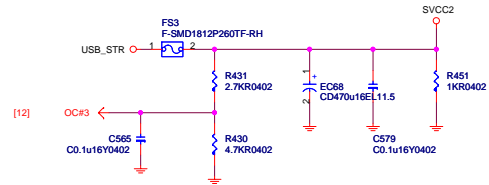
Close to LAN_Chip



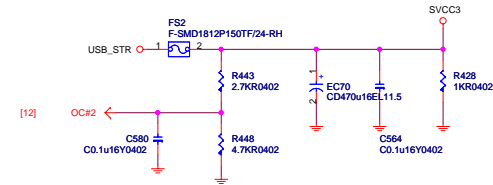
POWER CIRCUIT FOR USB PORT 0,1,2,3



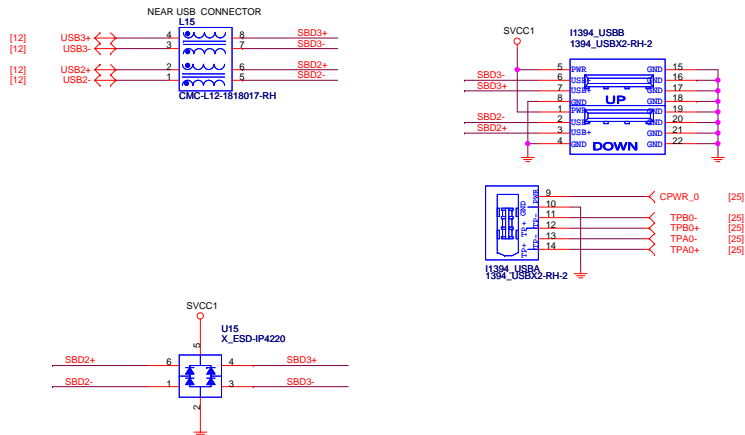
POWER CIRCUIT FOR USB PORT 4,5,6,7



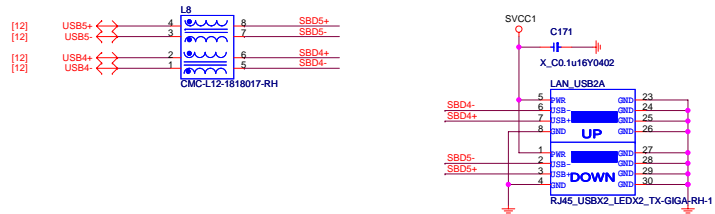
POWER CIRCUIT FOR USB PORT 8,9



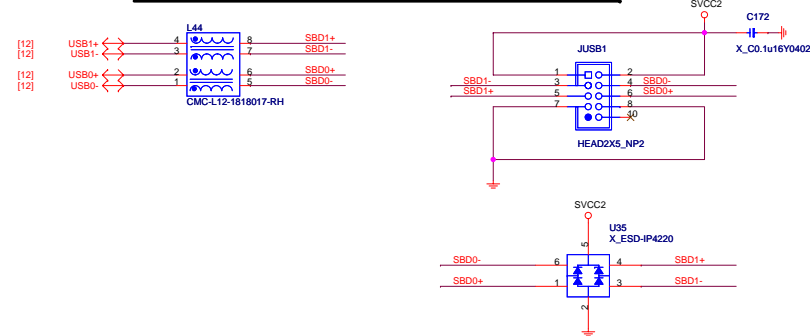
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



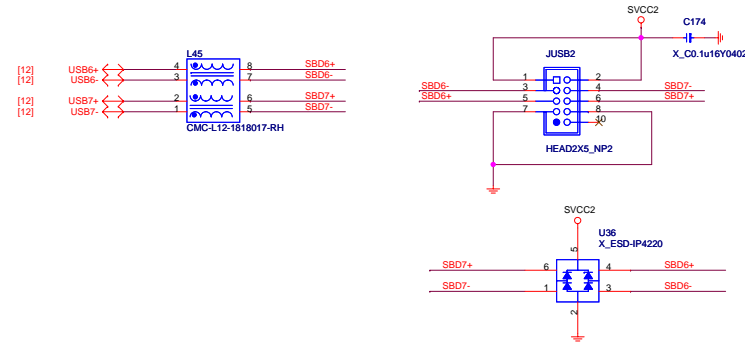
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



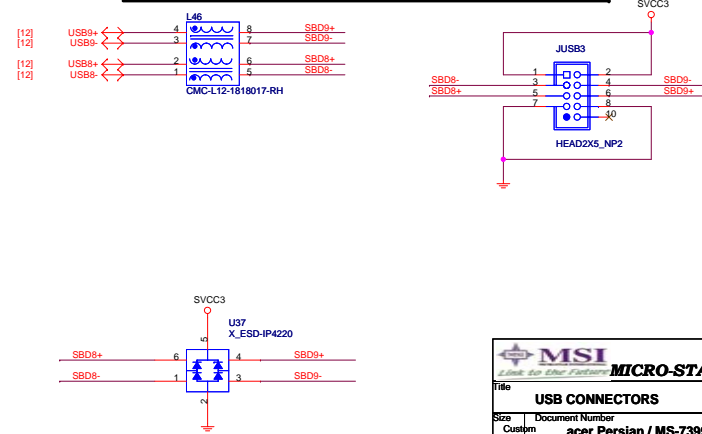
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

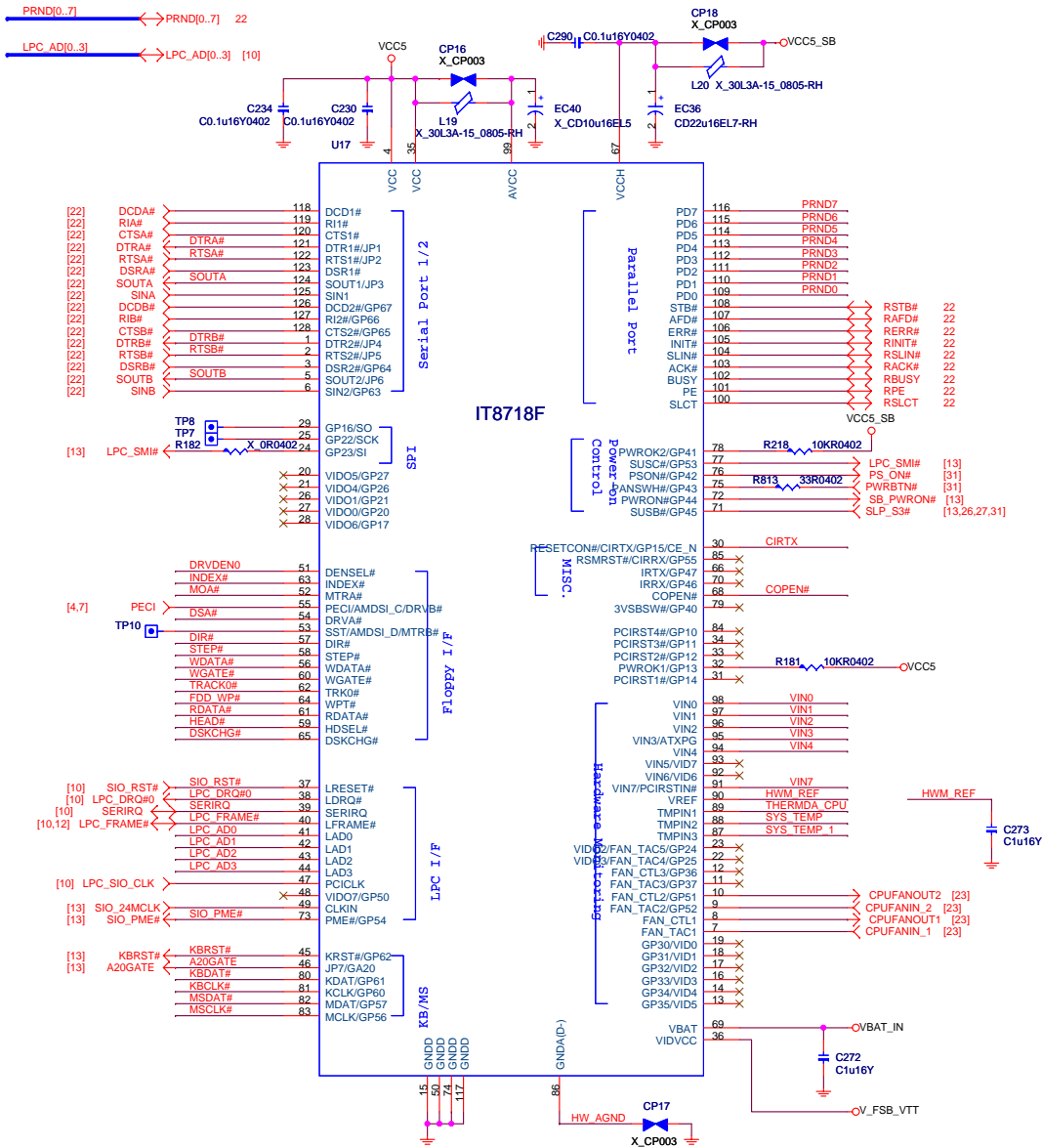


FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

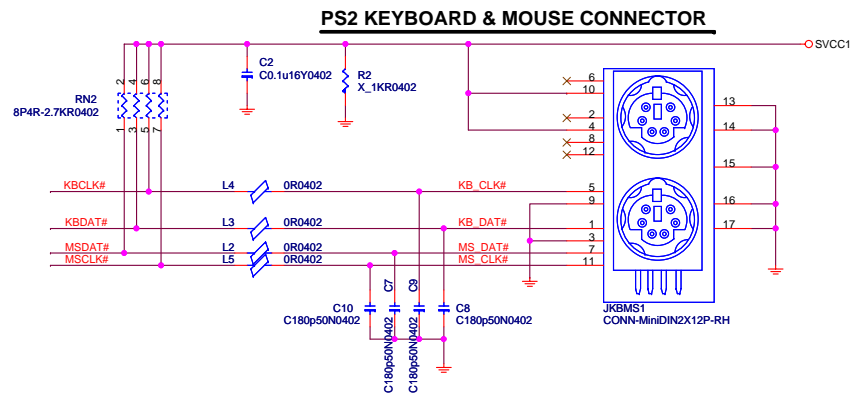


USB CARD READER + IR MODULE FOR USB PORT 8,9

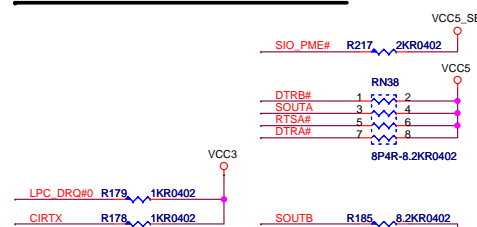




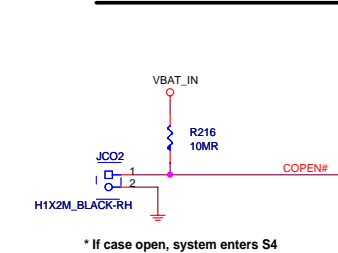
RTSB#	A20GATE	FAN DUTY
1	1	100%
1	0	75%
0	1	50%
0	0	25%



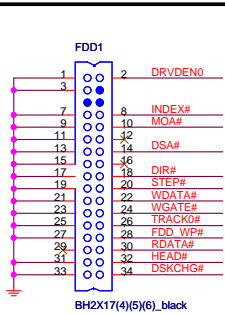
SUPER I/O STRAPPING RESISTOR



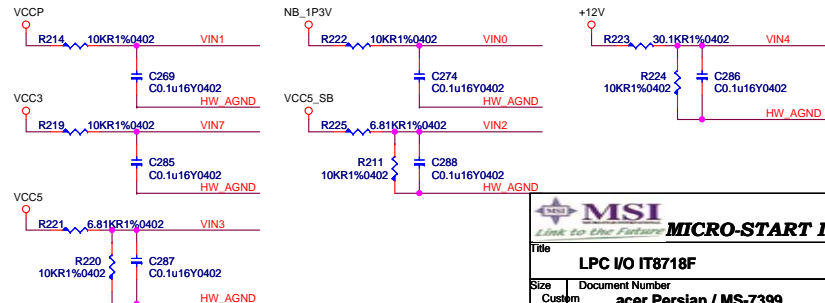
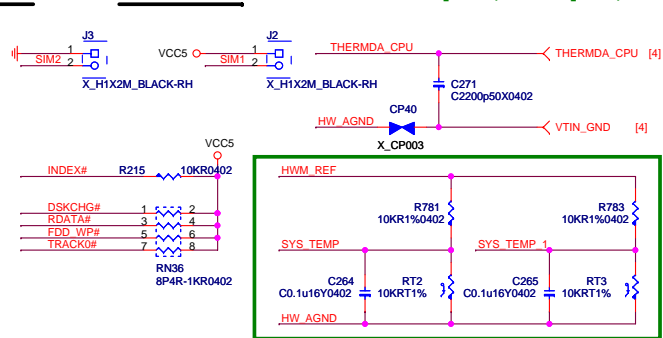
Chassis Intrusion



FLOPPY CONNECTOR

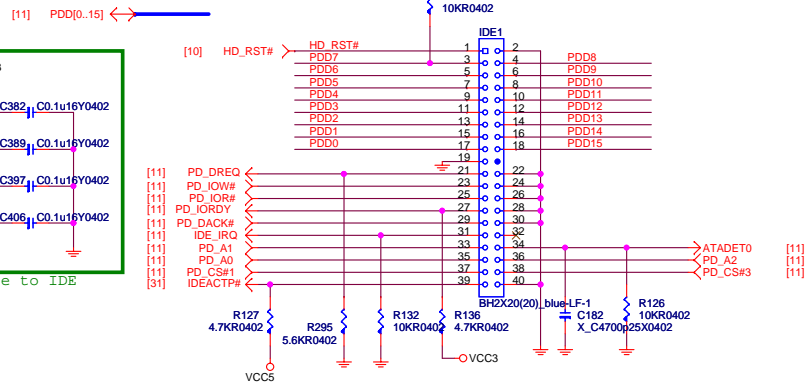


Simulation

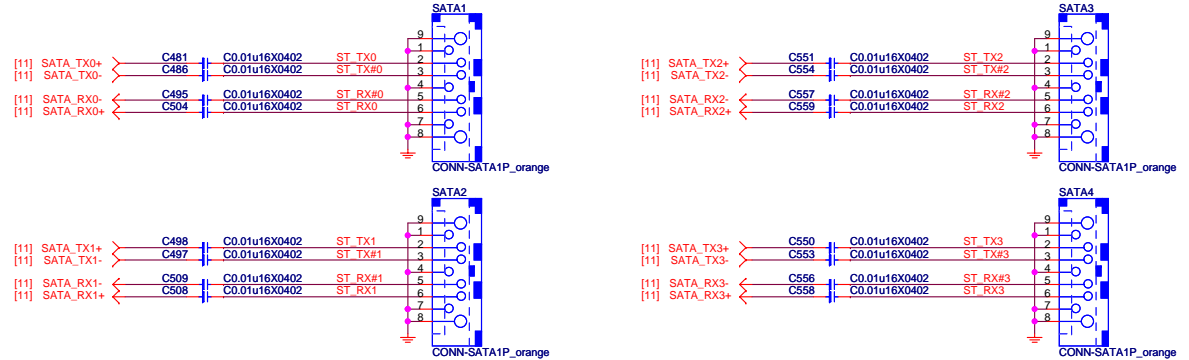


Title LPC IO IT8718F		
Size Custom	Document Number acer Persian / MS-7399	Rev 0A
Date: Thursday, August 23, 2007	Sheet 21	of 36

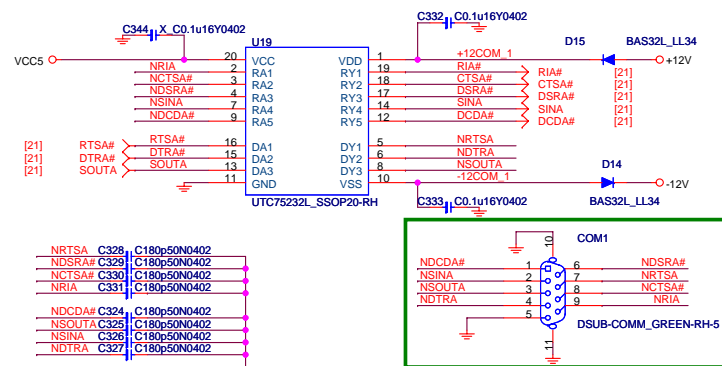
PRIMARY IDE BLOCK



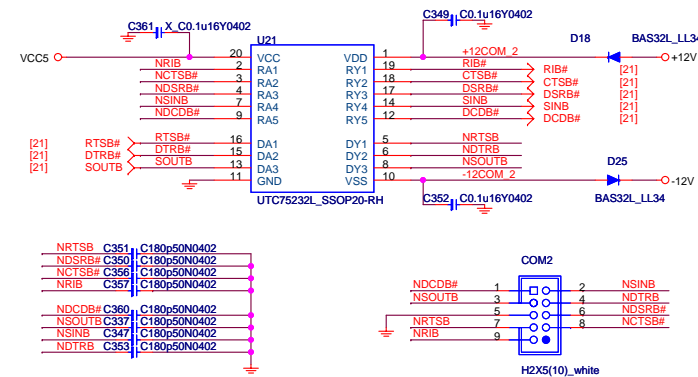
SERIAL ATA CONNECTOR BLOCK



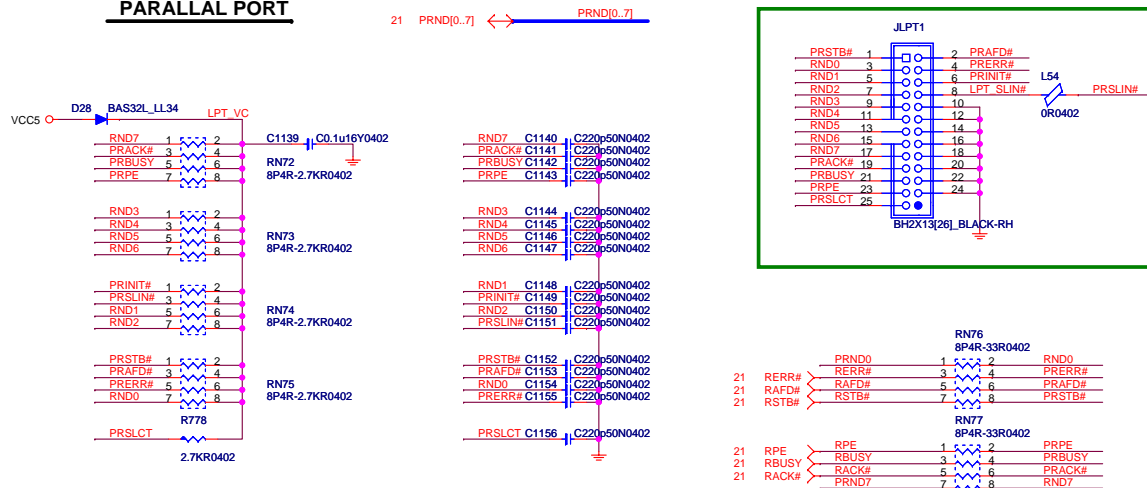
SERIAL PORT 1



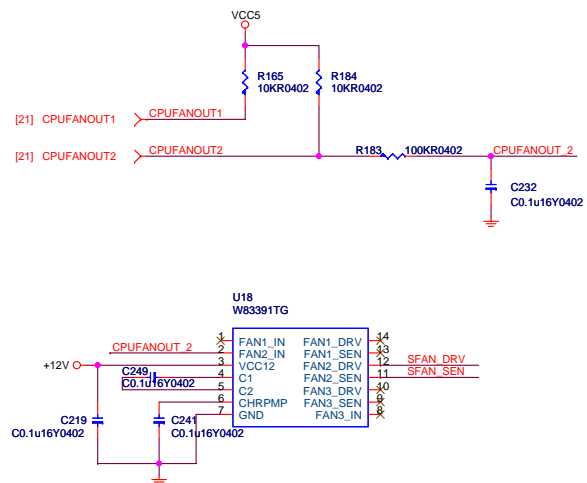
SERIAL PORT 2



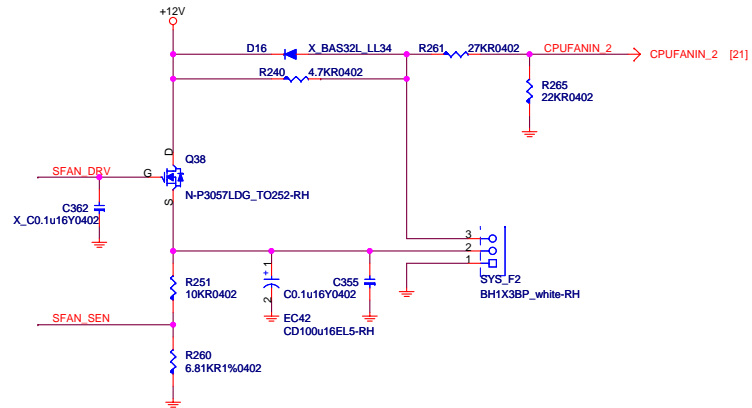
PARALLAL PORT



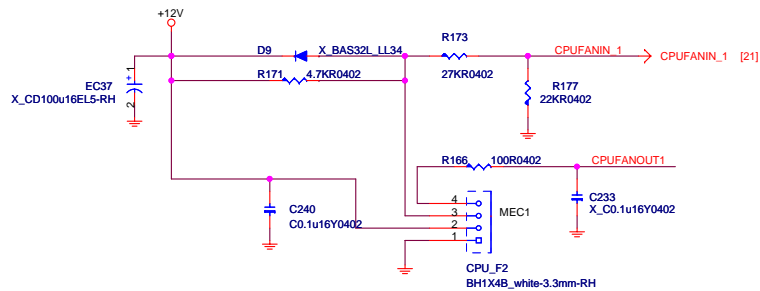
PWM FAN CONTROL



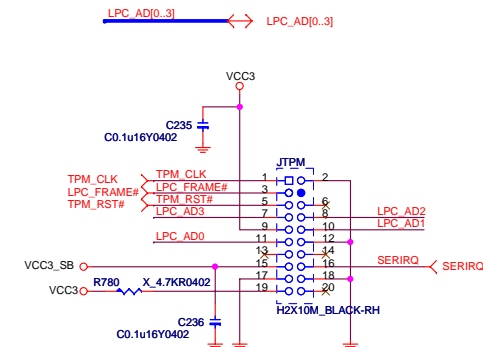
SYS FAN



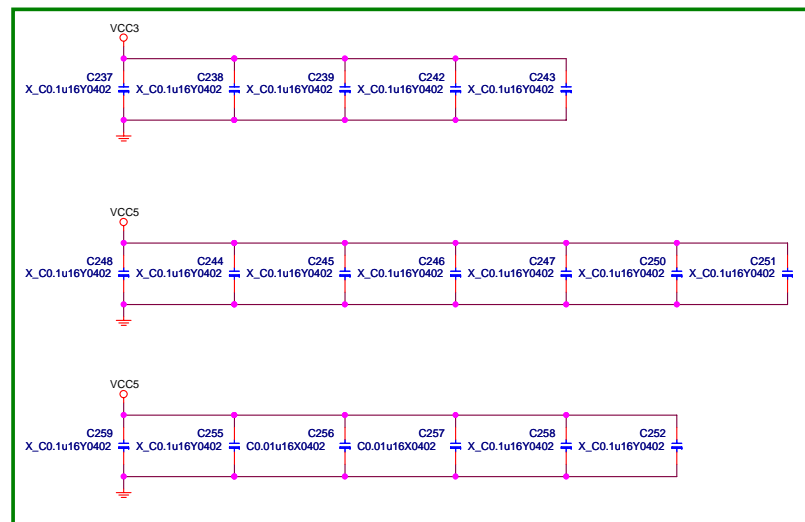
CPU FAN

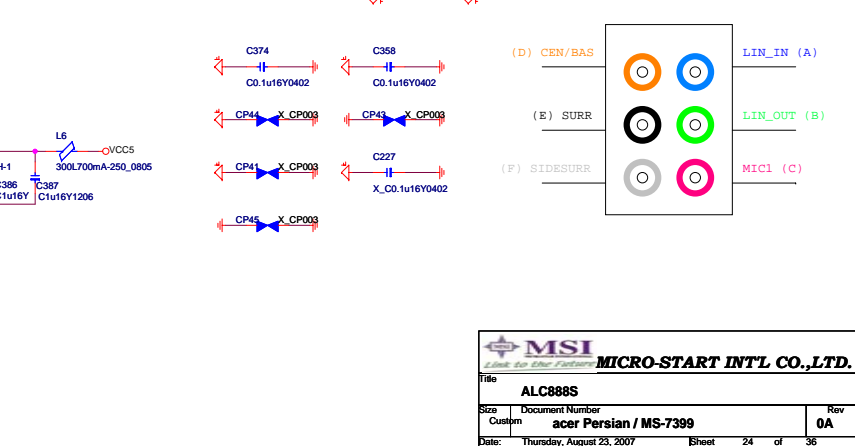
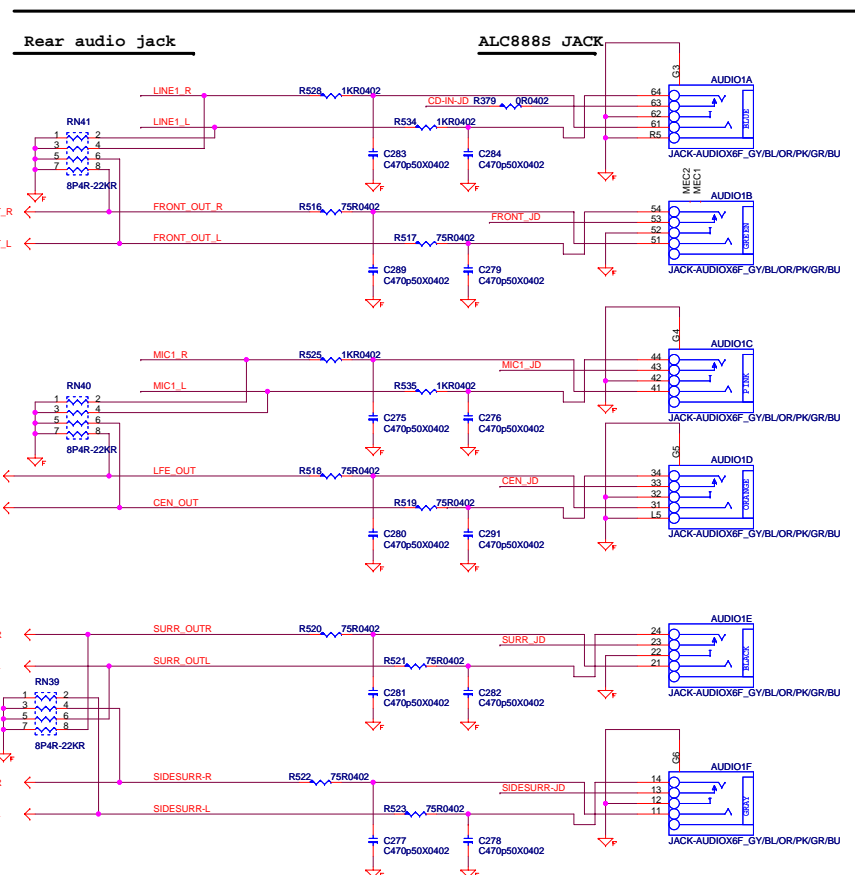
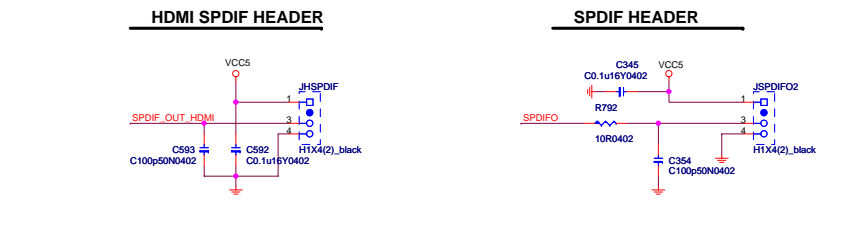
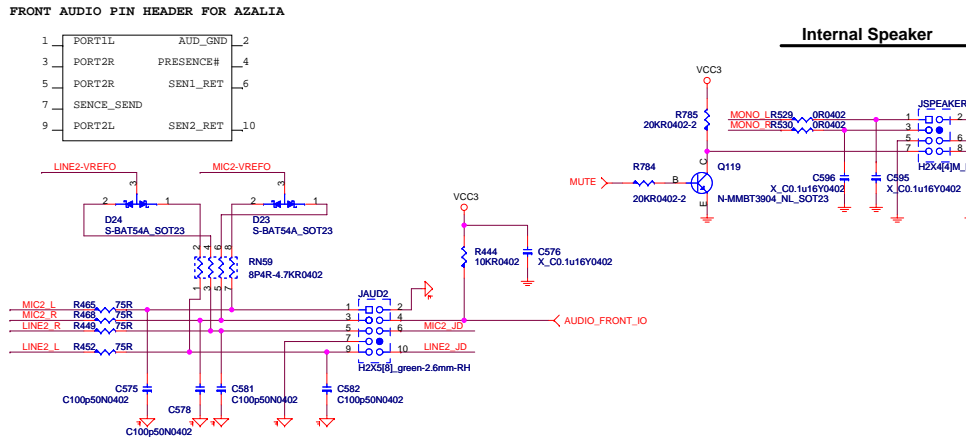
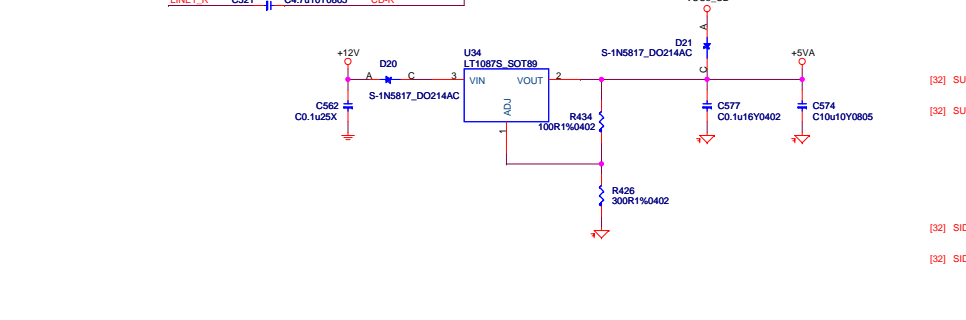
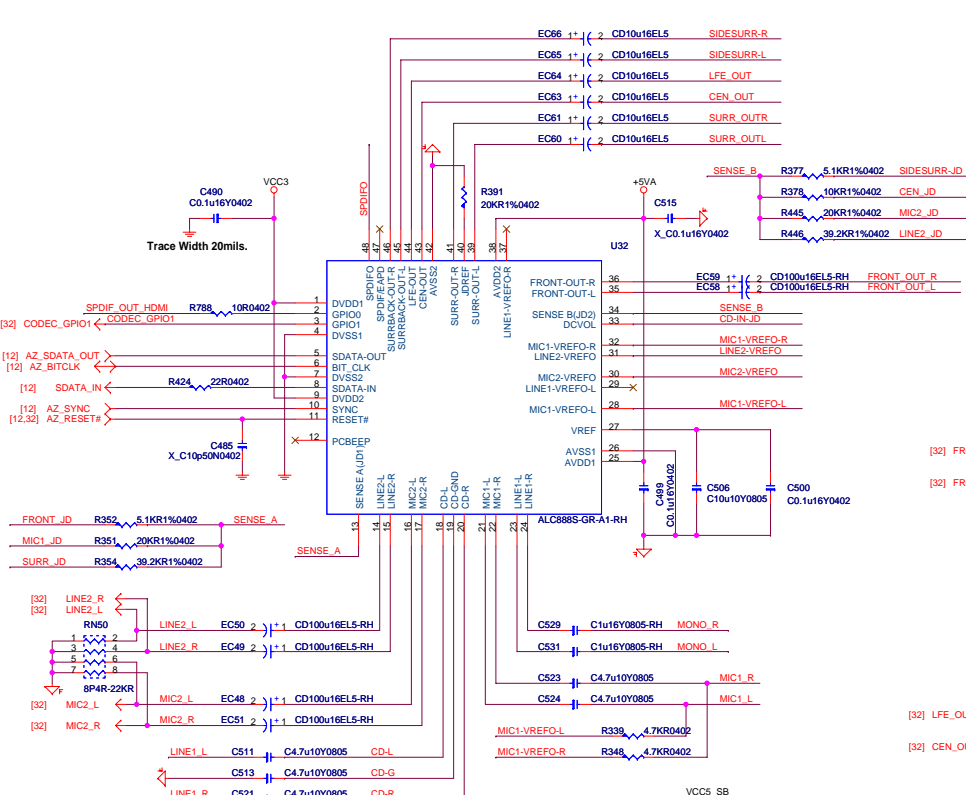


TPM Header



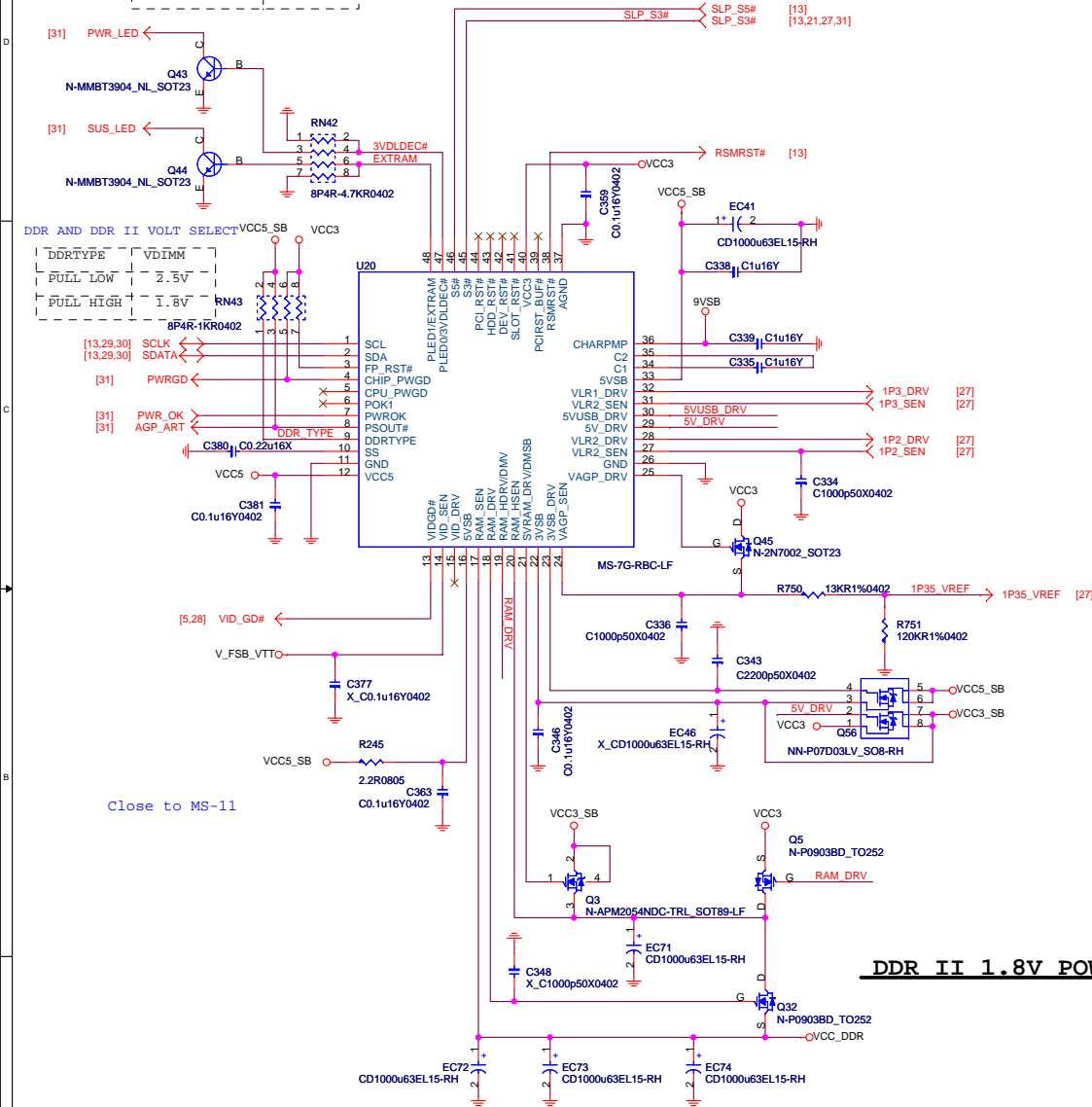
For EMI





3VSB MODE SELECT	
3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH



The schematic diagram illustrates a USB-to-serial interface circuit. It features two NPN transistors, Q62 (N-APM2054NDC-TRL_SOT189-LF) and Q75 (N-P0903BD_TO252), which act as level shifters. The circuit is powered by two 5V sources: 5V_USB_DRV and 5V_DRV. Decoupling capacitors C228, C555, C573, C208, and C211 are used to stabilize the power supply. Pull-up resistors R201 and R202 are connected to the USB_STR and USB_STR1 signals. The serial interface is connected to the bases and collectors of the transistors. The USB_STR signal is connected to the emitter of Q62 and the collector of Q75. The USB_STR1 signal is connected to the emitter of Q75 and the collector of Q62. The serial interface is connected to the bases of Q62 and Q75. The serial interface is connected to the bases and collectors of the transistors. The USB_STR signal is connected to the emitter of Q62 and the collector of Q75. The USB_STR1 signal is connected to the emitter of Q75 and the collector of Q62. The serial interface is connected to the bases of Q62 and Q75.

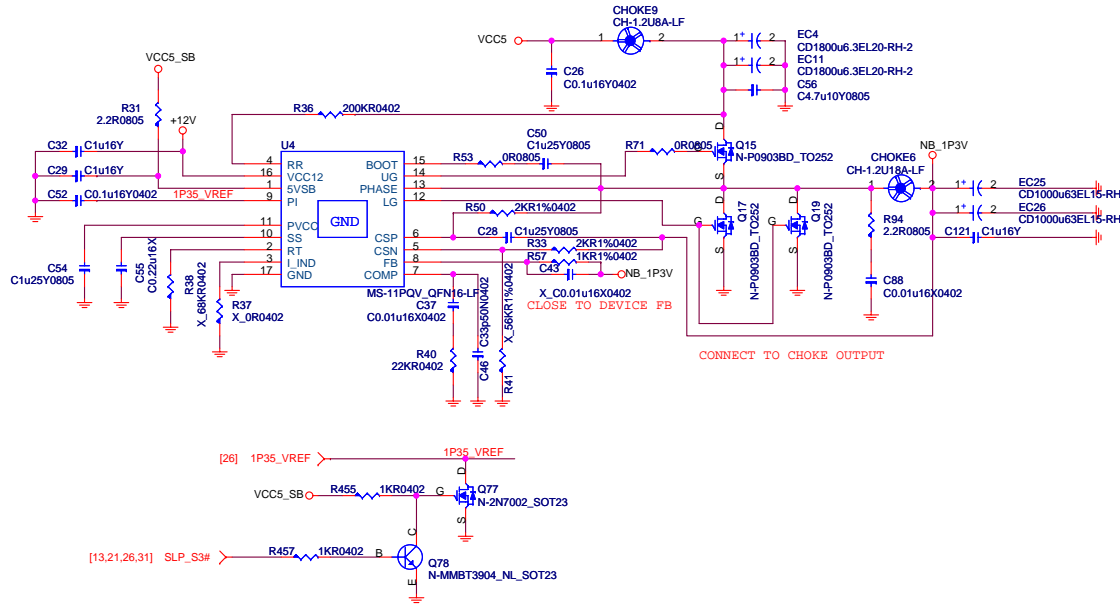
The schematic diagram shows the W83310DG SOP8-RH chip connected to various power supply rails. The chip's pins are labeled as follows: 1 (VIN), 2 (GND2), 3 (VREF1), 4 (VOUT), 5 (BOOT_SEL), 6 (VCTRL), 7 (ENABLE), 8 (VREF2), 9 (GND3), 10 (W83310DG), 11 (SOP8-RH), 12 (GND3), 13 (GND3), 14 (GND3), 15 (GND3), 16 (GND3). The chip is connected to VCC3_SB, VCC_DDR, VTT_DDR, VCC5, and VCC3. Decoupling capacitors include C225, C226, EC30, EC32, C214, EC45, and EC57. Resistors include R163 and R170. The chip is connected to a CD1000u63EL15-RH capacitor.

NB 1.3V CORE POWER

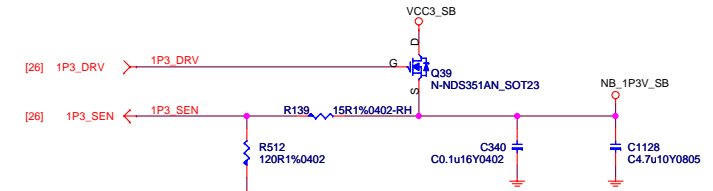
(1.3V--8.776A+V_FSB_VTT---5.6A=14.376)

The Ripple Current For V_1P25_CORE:
 $Duty = (1.35V/5V) * (100\%/80\%) = 0.3375$ (Efficiency: 80%)
 $I_{rms} = I_o * \{ [Duty * (1 - Duty)]^{0.5} \}$
 $= 14.4 * \{ [0.27 * 0.73]^{0.5} \} = 6.393 (A)$

Rated Ripple Current (65 degree): $1800mA * 2.3 * 2 = 8.28A > 6.393A$

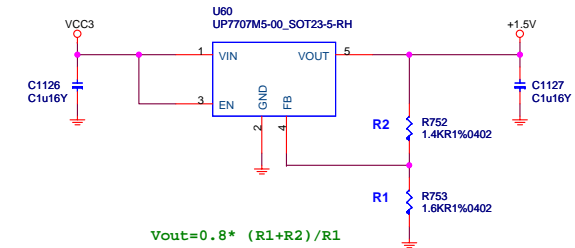


NB 1.3VSB POWER 25mA

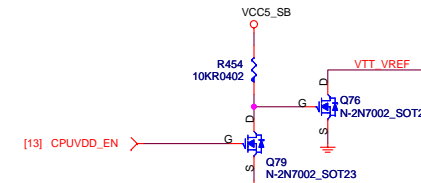
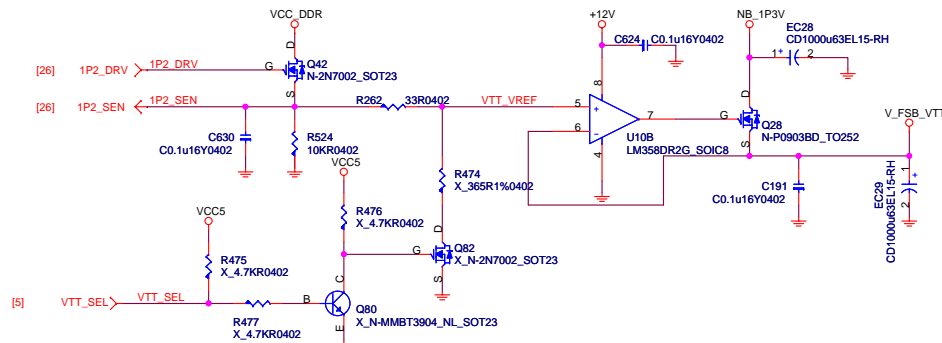


+1.5V POWER

up7707: 600mA Low Dropout Linear Regulator

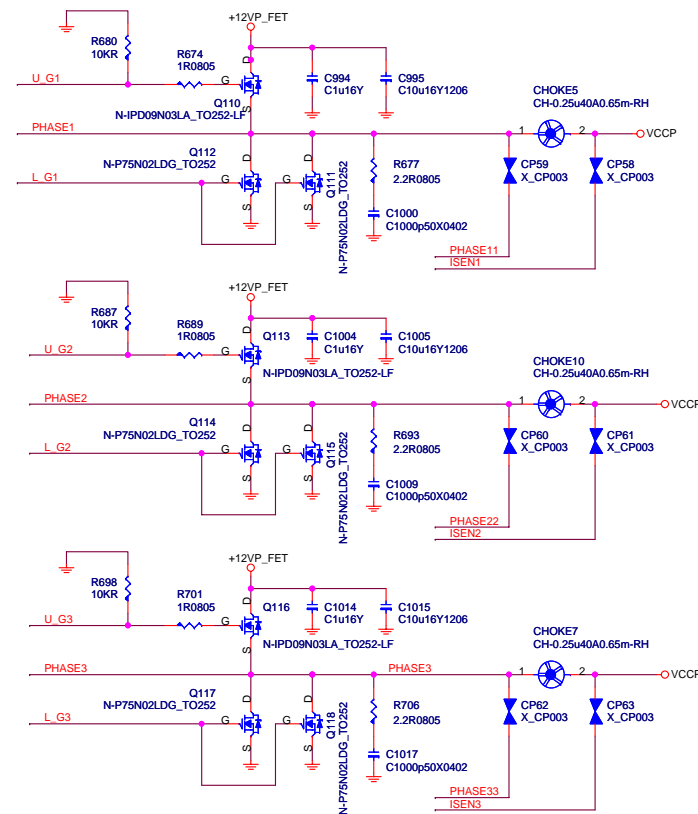
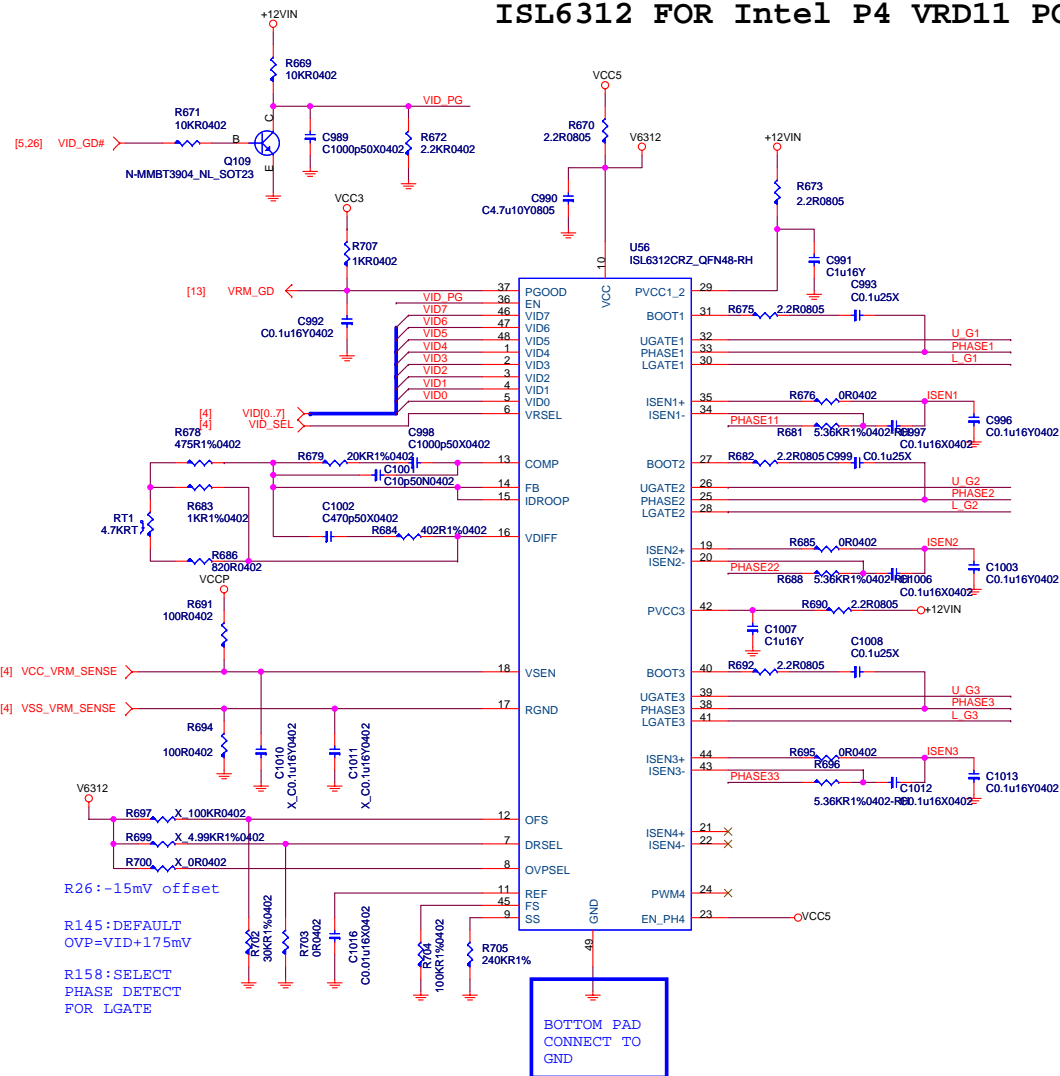


CPU FSB VTT POWER

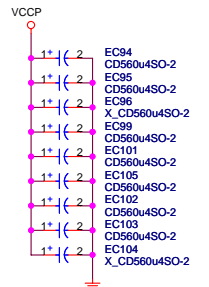


VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

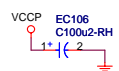
ISL6312 FOR Intel P4 VRD11 POWER CKT



OS-CON Capacitors

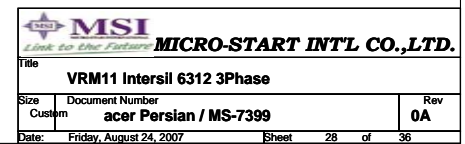
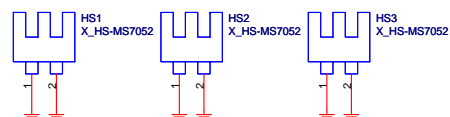
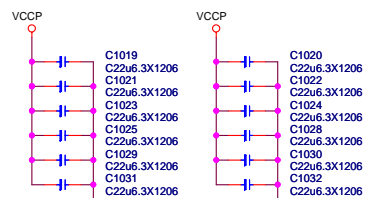
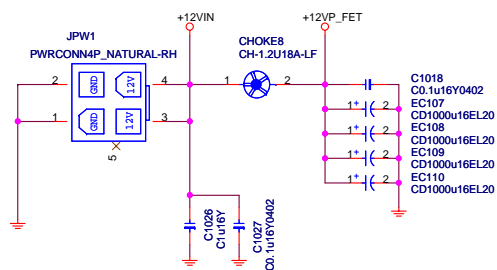


SP Capacitors

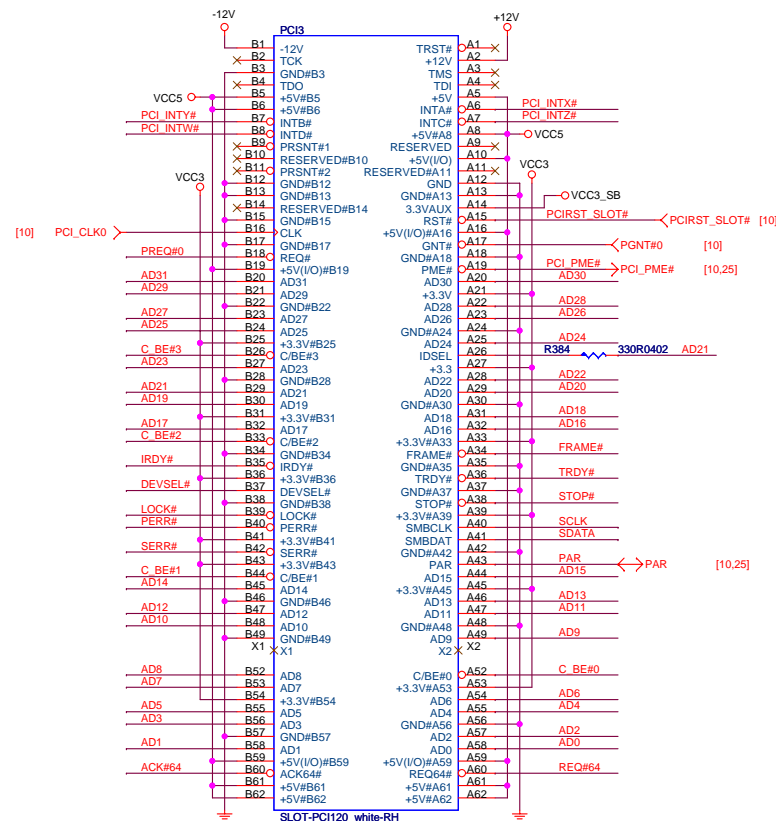


CPU DECOUPLING CAPACITORS

Place these caps within socket cavity

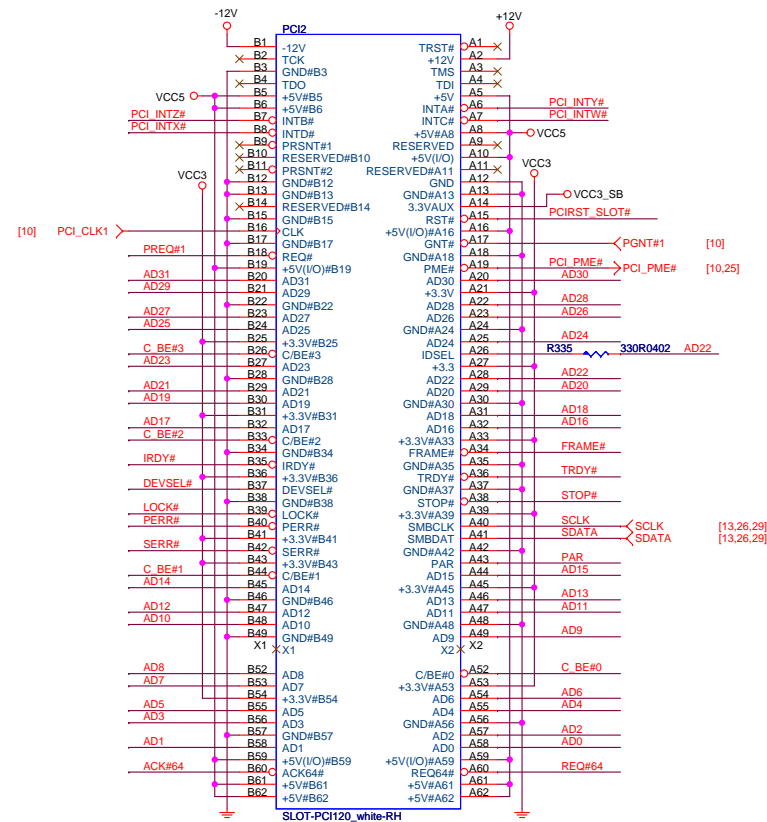


PCI SLOT 1 (PCI VER: 2.3 COMPLY)



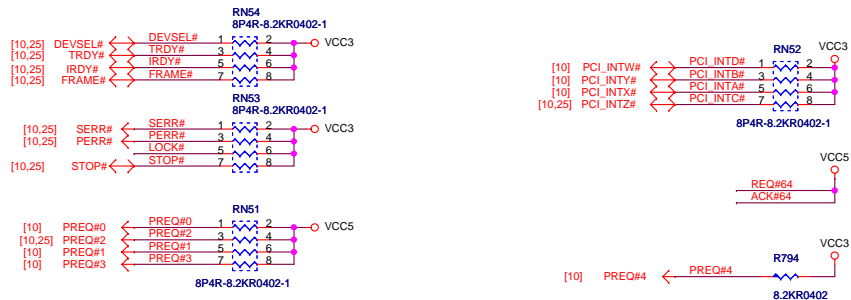
IDSEL = AD21
MASTER = PREQ#0
PCI_INTX#

PCI SLOT 2 (PCI VER: 2.3 COMPLY)

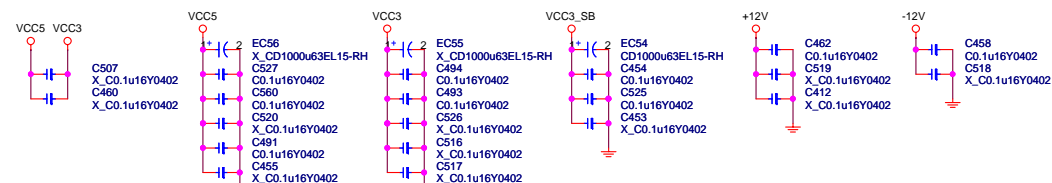


IDSEL = AD22
MASTER = PREQ#1
PCI_INTX#

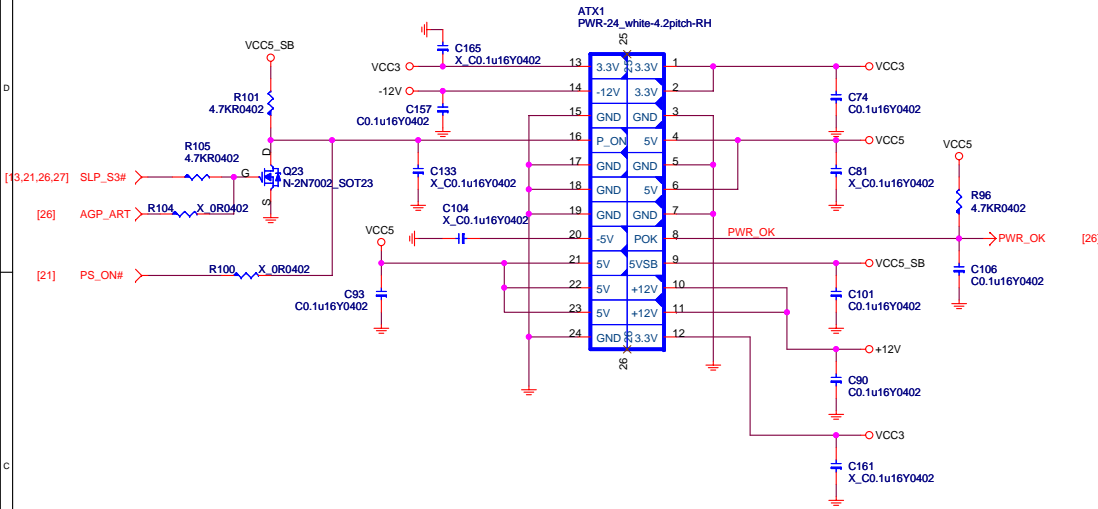
PCI PULL-UP / DOWN RESISTORS



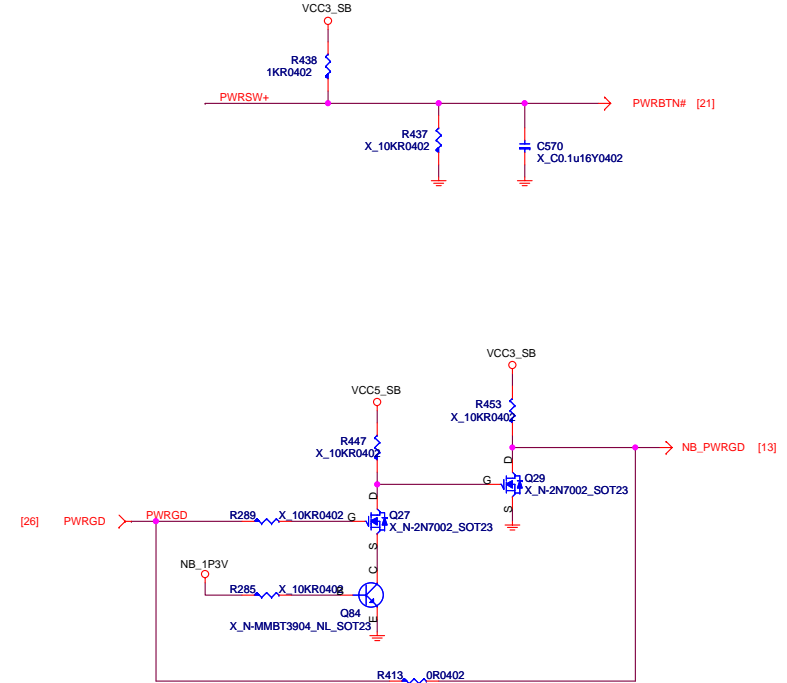
PCI SLOT DECOUPLING CAPACITORS



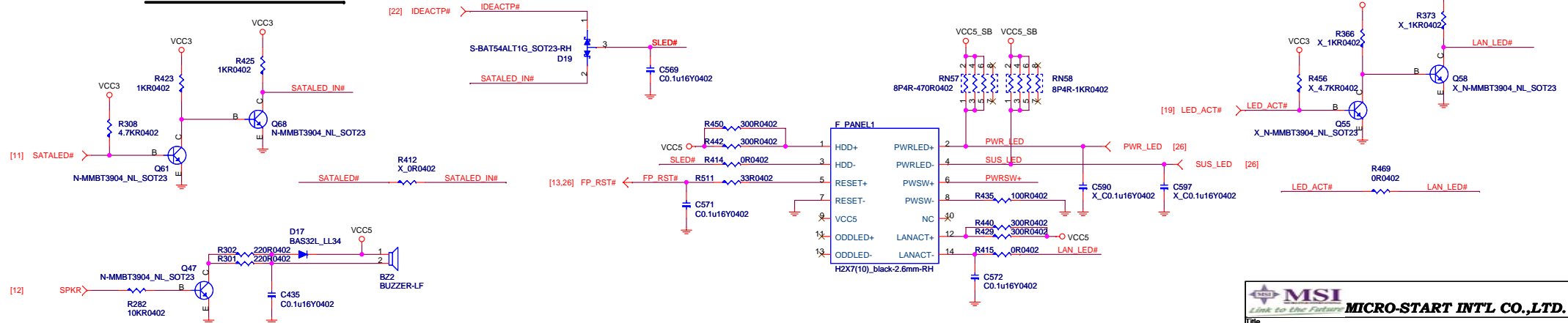
ATX CONNECTOR



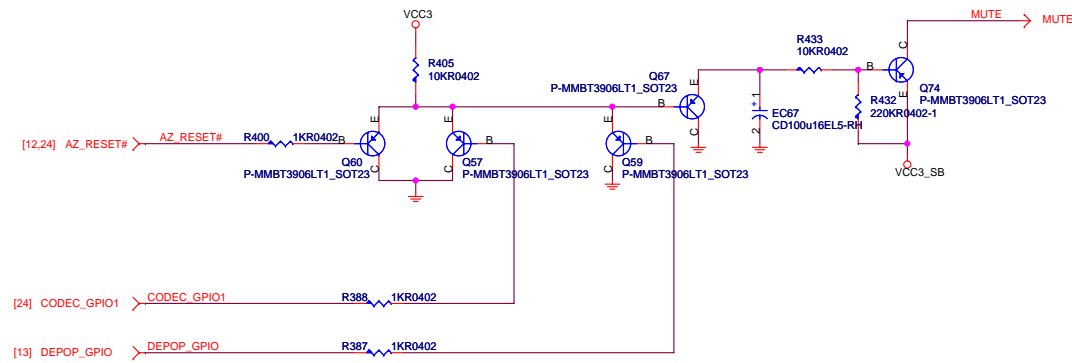
POWER BUTTON



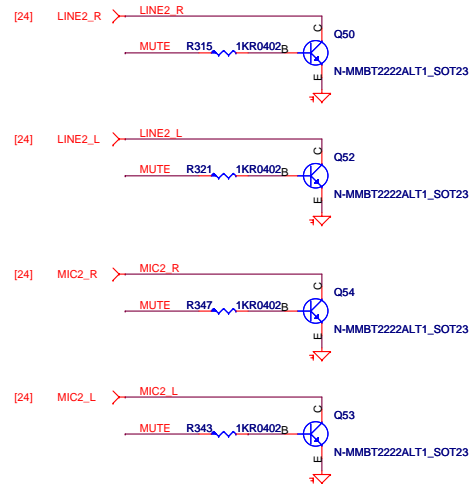
acer Front Panel Connector



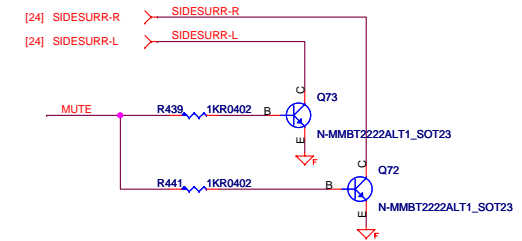
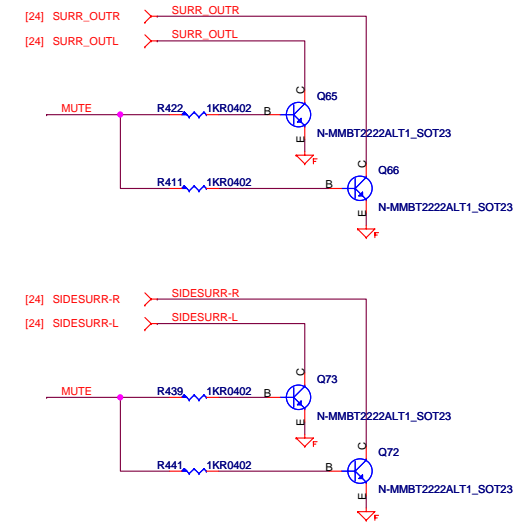
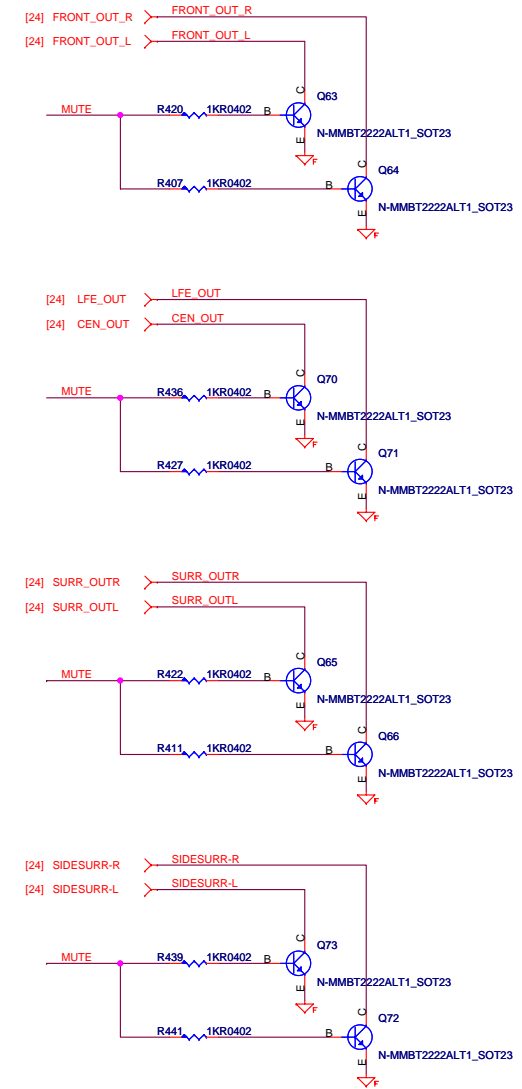
Audio De-Pop Control Circuit



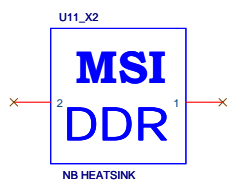
Front Audio Port De-Pop Circuit



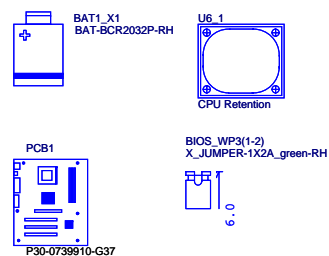
Rear Audio Port De-Pop Circuit



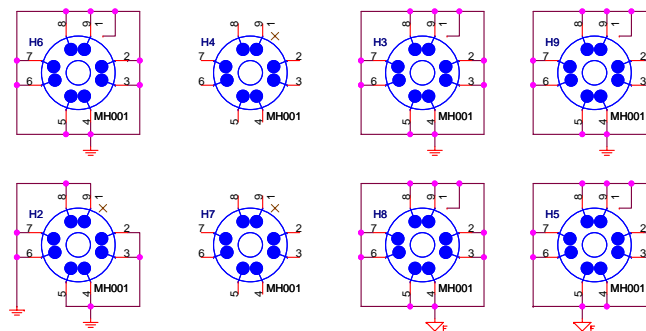
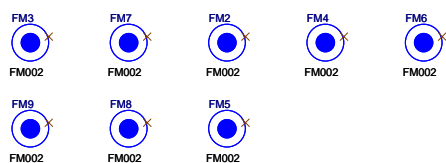
HEAT SINK

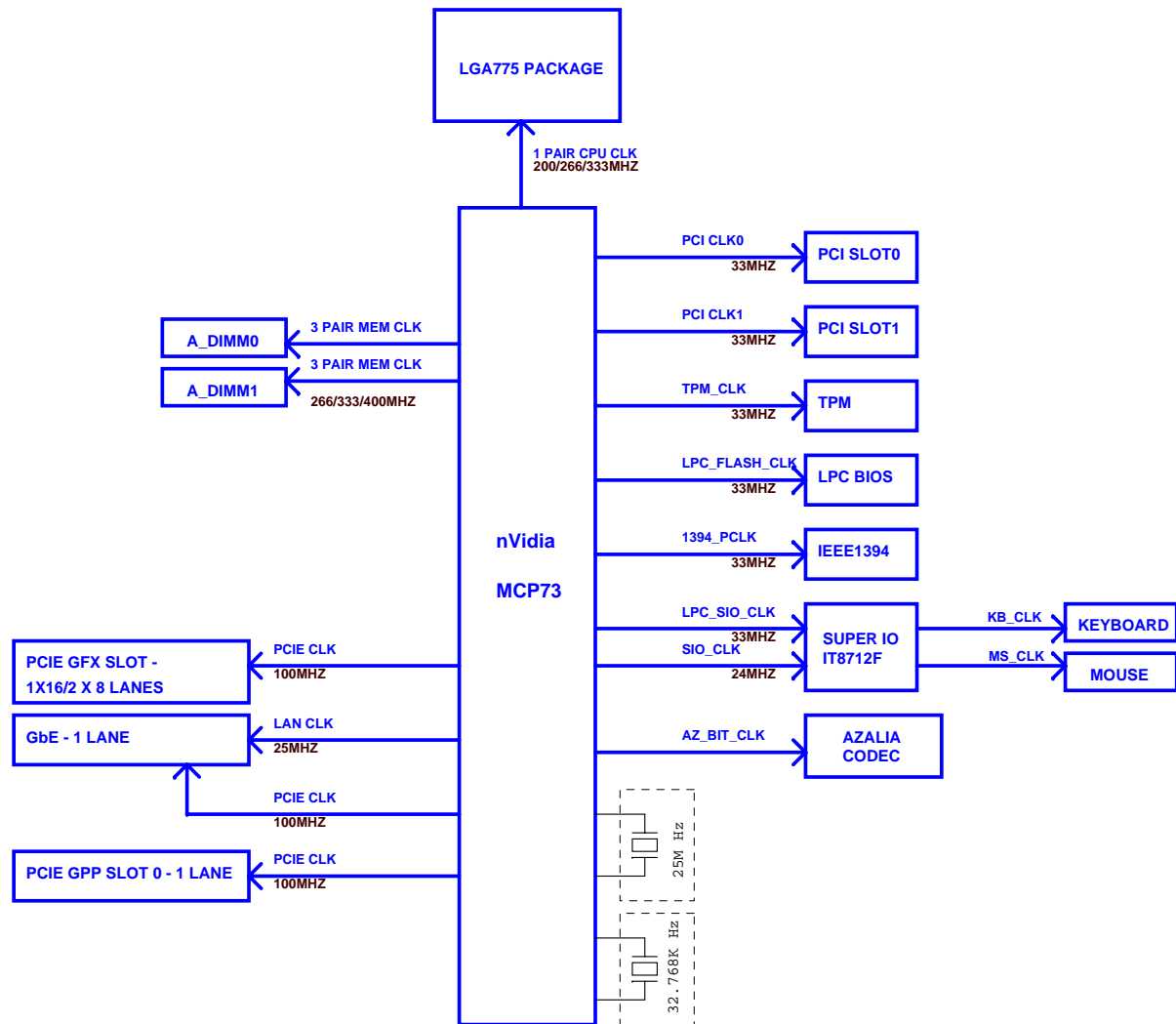


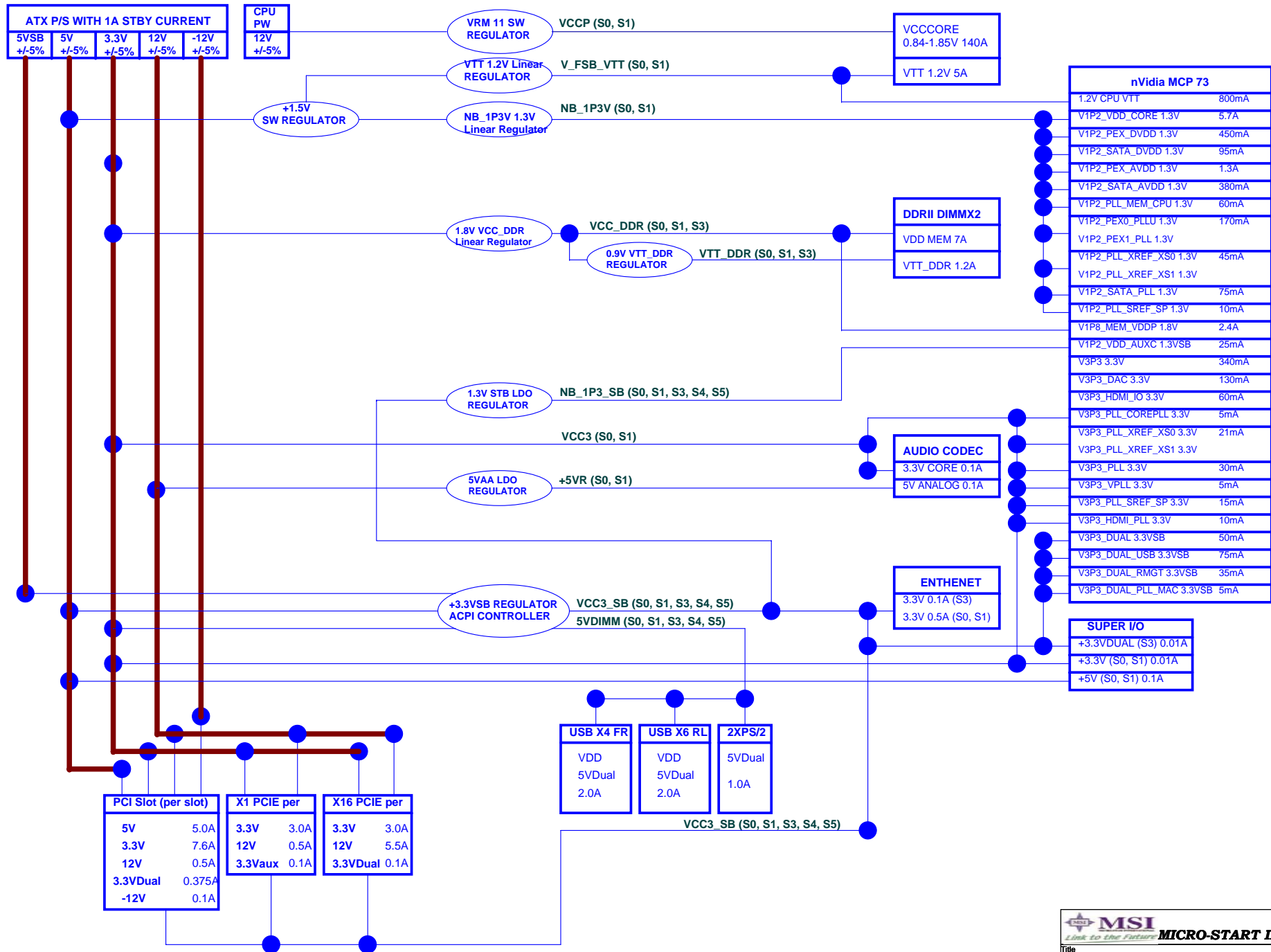
MANUAL PART

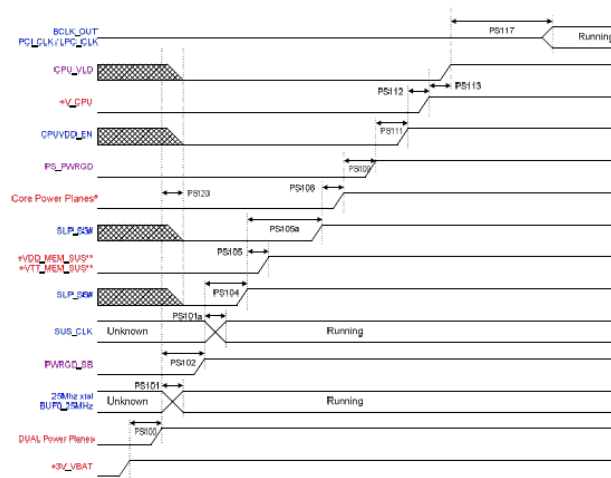


Optics Orientation Holes







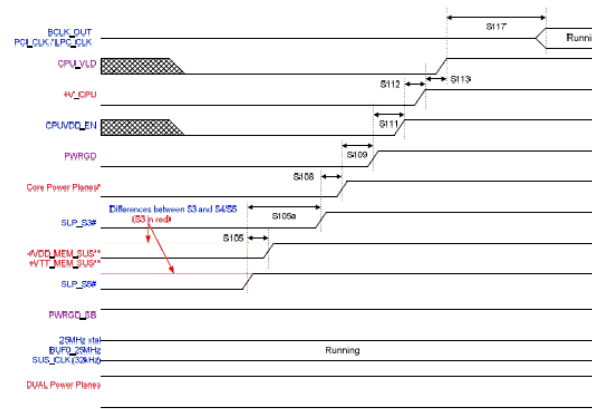


Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

* Core Planes include:
All power planes without _DUAL or _SUS in the name except:
CPU Core Power Plane

** DDR2 Memory Power Planes:
VDD = 1.8V
VTT = 0.9V

MCP73 G3-to-S0 Power-Up Sequence

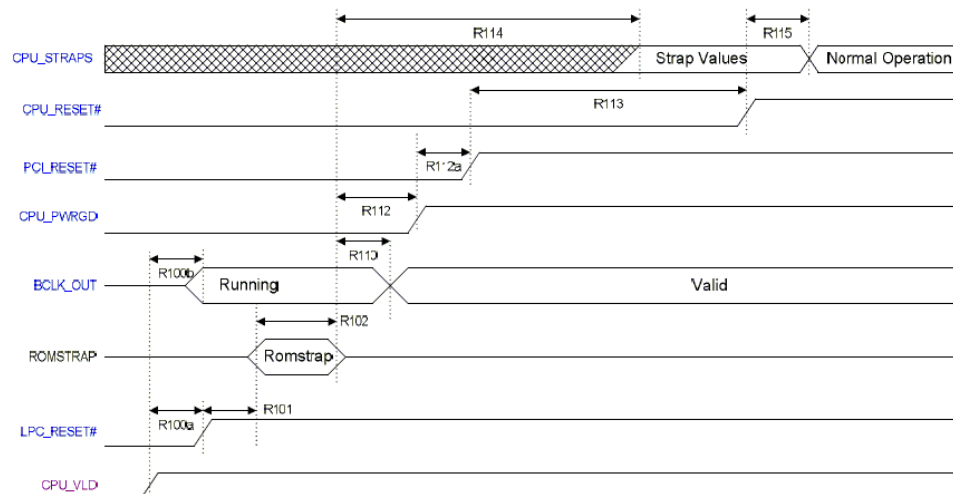


Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

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All power planes without _DUAL or _SUS in the name except:
- CPU Core Power Plane

** DDR2 Memory Power Planes:
VDD = 1.8V
VTT = 0.9V

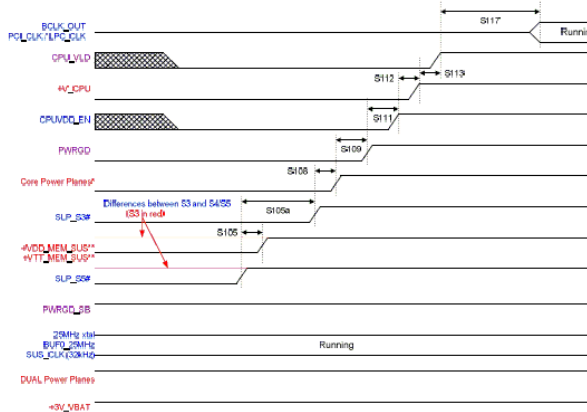
MCP73 S3/S4/S5 to S0 Power Resume Sequence



MCP73 output signals in Blue

Motherboard generated signals in Purple

MCP73 Cold Reset Power-Up Sequence



Power Planes in Red MCP73 output signals in Blue Motherboard generated signals in Purple

* Core Planes include:
All power planes without _DUAL or _SUS in the name except:
- CPU Core Power Plane

** DDR2 Memory Power Planes:
VDD = 1.8V
VTT = 0.9V

MCP73 S3/S4/S5 to S0 Power Resume Sequence